An Ultra Low Noise High Speed CMOS Linescan Sensor for Scientific and Industrial Applications

Boyd Fowler*, Janusz Balicki*, Dana How*, Steve Mims*, John Canfield, and Michael Godfrey

*Agilent Technologies
previously Pixel Devices Intl. Inc.

ABSTRACT

This paper describes a 2048×1 linear image sensor implemented in a 0.35μm 1P4M CMOS process that uses a low fixed pattern noise capacitive transimpedance amplifier (LFPN CTIA) pixel architecture. The pixel also includes circuitry for correlated double sampling, electronic shuttering, and a horizontal anti-blooming drain. High speed non–destructive read–out of the sensor is achieved by using a hierarchical read–out structure with two output ports. Using a JTAG interface the sensor can be programmed to operate in multiple read–out modes. In the fastest read–out mode, ROI, the sensor achieves 90Mpixel/sec (43.4Klines/sec) with 14e- RMS read noise. In the lowest noise mode, MRDI, with 13x oversampling of each pixel the sensor achieves 2.7Klines/sec with 1.2e- RMS read noise.

Keywords: Linescan, CTIA, low noise, CMOS image sensors, APS

1. INTRODUCTION

Presently, CMOS image sensors compete favorably with CCDs in consumer applications such as cell phones and PC cameras, but there is still a misconception that they are too noisy and lack the sensitivity of CCDs for most industrial and scientific products. In this paper we present results from a linear CMOS image sensor that out–performs the best scientific and industrial linear CCD image sensors available in the market today.[1,2] Although CMOS image sensors may never replace CCDs in every application we will show that when high speed, high sensitivity, and low noise are needed together CMOS image sensors offer a clear advantage over CCDs.[3]

This paper describes a 2048×1 linear image sensor (LNL2048SC) implemented in a twin well 8μm p- epi 0.35μm 1P4M CMOS process that uses a low fixed pattern noise capacitive transimpedance amplifier (LFPN CTIA) pixel architecture.[4] The pixel also includes circuitry for correlated double sampling, electronic shuttering, and a horizontal anti-blooming drain. High speed non–destructive read–out of the sensor is achieved by using a hierarchical read–out structure with two output ports. Using a JTAG interface the sensor can be programmed to operate in multiple read–out modes. In the fastest read–out mode the sensor achieves 90Mpixel/sec (43.4Klines/sec) with 14e- RMS read noise. In the lowest noise mode with 13x oversampling of each pixel the sensor achieves 2.7Klines/sec with 1.2e- RMS read noise. This oversampled line rate is based on reading out the same line 13 times at 80Mpixel/sec.

This paper is organized as follows: Section 2 describes the circuitry and operation of the LNL2048SC sensor, and Section 3 presents measured results from the sensor and compares them with our initial design goals. Finally in Section 4 we discuss how this sensor compares with recently published sensors.

2. LNL2048SC SENSOR

In this section we describe the operation and circuitry of the LNL2048SC sensor. The LNL2048SC was designed in a 0.35μm 1P4M CMOS process with twin wells on 8μm p- epi. The sensor was designed to use a single 3.3±0.3V power supply.

Corresponding author information: email: boyd_fowler@agilent.com; phone: 408-970-2801; fax: 408-970-2416;

2.1. Sensor Architecture

The block diagram for the LNL2048SC sensor is shown in Figure 1. The sensor contains three main blocks: the digital control block, the 2048×1 pixel array with associated amplifiers and shift registers, and the output buffers. The digital control block has a JTAG interface that allows the sensor to be operated in four simple internal control modes and one externally controlled mode. The digital block also controls the electronic shuttering of the pixels. The logic design minimizes switching during photocharge integration and therefore reduces any coupling noise between the digital logic and the pixels. The pixel array contains 2048×5 photodiodes where only the center 2048×1 photodiodes are light sensitive. The other dummy photodiodes are used to improve the uniformity of the sensor. The pixel array is arranged for two port read–out, where the even pixels (0,2,4,6, ...) are read out of one port and the odd pixels (1,3,5,7, ...) are read out of the other port. There is one shift register for reading out the even pixels and one for reading out the odd pixels. Both shift registers are controlled by the digital control block. The gain of each pixel can be independently programmed to be either 1 or 10 using the gain shift register. In this paper we will only discuss operation in the 10 gain mode. The pixel array also contains a hierarchical analog multiplexer that enables high speed read–out of the sensor. The output buffers produce the final analog data (AEP, AEN, AOP, AON) and are designed to drive a 50pF/1KΩ parallel load at 50MHz. They are controlled by the digital logic and can be powered down whenever pixel data is not being read out. In addition, the odd and even pixel data can be multiplexed onto one output port for lower speed applications.*

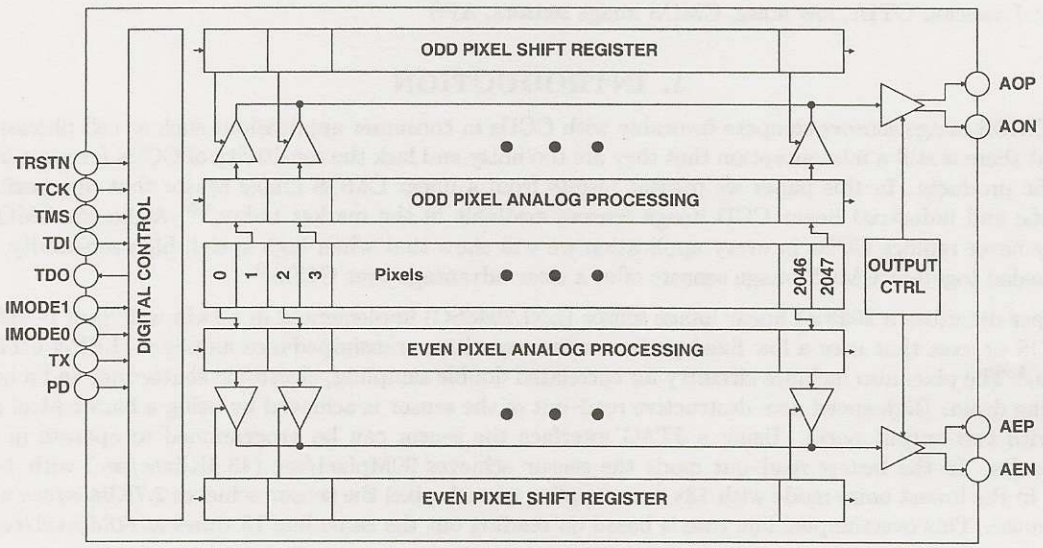

Figure 1. Sensor Block Diagram

2.2. Pixel Operation

A schematic of the pixel is shown in Figure 2. The pixel consists of three components, an n–well/p–substrate photodiode, an LFPN CTIA, and a capacitive sampling network. The photodiode is implemented using an n–well diffusion into the p–substrate. The bounding box of the nwell photodiode is 3μm×6μm with the corners cut off at a 45 degree angle (making the pixel an octagon). The pitch between pixels is 7μm. The pitch between pixels and dummy photodiodes is 9.7μm. The n–well is pulled back 1.0μm from the adjacent p–well to help reduce the photodiode capacitance and increase the UV/blue responsivity of the sensor by depleting more of the silicon surface. Although the gap between the n–well and p–well reduces the read noise and increases the UV responsivity of the sensor it also increases the leakage current of the sensor due to surface leakage. This tradeoff was selected because responsivity and read noise are much more important than leakage current in high speed linescan applications.

*This feature is not shown in the block diagram.

The LFPN CTIA fixes the voltage across the photodiode and integrates the photon induced charge on the capacitive feedback network **C1**, **C2**, and **C3**. **RESET** controls an NMOS transistor and **RESET2** controls a CMOS switch. In this paper we define a CMOS switch as an NMOS and a PMOS transistor in parallel, i.e. a CMOS pass gate. The LFPN CTIA is reset by pulling **RESET** and **RESET2** high. After reset is complete **RESET2** falls to ground and then **RESET** falls slowly to approximately 0.5 volts. The slower **RESET** falls the smaller the reset noise. Since **RESET** falls to only 0.5 volts, the NMOS reset transistor on the LFPN CTIA acts as a horizontal anti–blooming drain up to the bias current of the pixel amplifier. **LS** controls a CMOS switch that either connects or disconnects **C4** from the output of the pixel amplifier. Capacitor **C4** is used to bandlimit the pixel amplifier. The value of **C4** is approximately 1pF.

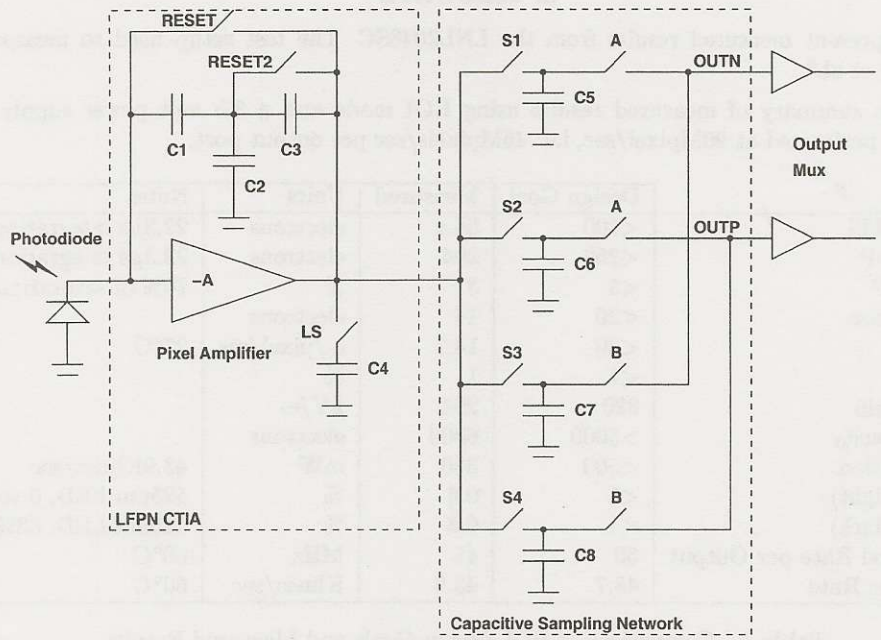

Figure 2. Pixel Schematic

The capacitive sampling network is used to both sample data and bandlimit the LFPN CTIA. The four capacitors **C5**–**C8** are designed to be approximately 1pF and the CMOS switches controlled by **S1**, **S2**, **S3**, and **S4** can be operated in any order. The CMOS switches controlled by **A** and **B** are used to bank switch the capacitors for double buffered read–out operation. These capacitors can also be used to perform correlated double sampling (CDS) of the LFPN CTIA to reduce reset noise. Although CDS reduces reset noise, it also reduces the speed of the LFPN CTIA, therefore CDS is not used in the highest speed mode of operation.

The pixel circuitry can be operated in many different modes using the JTAG interface. The two modes of operation that will be reported in this paper are read on integration (ROI) and multiple read–outs during integration (MRDI). ROI is the fastest mode of operation for the sensor. In this mode of operation **C6** and **C8** are used to double buffer the pixel data, **LS** is low (i.e. **C4** is disconnected from the output of the pixel amplifier) to increase the bandwidth of the pixel amplifier, and CDS is not performed. Moreover, when the pixel level amplifier is connected to **C6**, **C8** is being read out, and on the next line **C8** is connected to the pixel level amplifier and **C6** is being read out. MRDI is the lowest read noise mode of operation for the sensor. In this mode **C4**, **C5**, **C6**, **C7**, and **C8** are always connected to the output of the pixel amplifier and **LS** is high, bandlimiting the amplifier and reducing its noise. In addition, MRDI reduces noise by using multiple samples of each pixel on each line.[6–8]

2.3. Readout Operation

The read–out circuit is composed of a two level hierarchical buffered multiplexer and is controlled by the read–out shift register. Pixel data is multiplexed 64 to 1 and then 16 to 1 to produce the final output data. At each level of the hierarchy a standard 5 transistor NMOS input differential amplifier was used to buffer the pixel data. The structure of the hierarchy was selected to optimize the sensor speed while minimizing the read–out noise. The read–out multiplexer produces a differential output signal (AEP/AEN or AOP/AON) from a differential input signal (OUTP/OUTN), but in both ROI and MRDI modes of operation the output is single–ended. The 3db bandwidth and the output referred RMS noise of the read–out multiplexer were designed to be 81MHz and 69μV respectively.

3. RESULTS

In this section we present measured results from the LNL2048SC. The test setup used to measure this data is described by Fowler et al.[9]

Table 1 shows a summary of measured results using ROI mode and a 3.5 volt power supply. All of these measurements were performed at 90Mpixel/sec, i.e. 45Mpixels/sec per output port.

	Design Goal	Measured	Units	Notes
Offset FPN RMS	<100	54.4	electrons	22.3μs integration time
Offset FPN P-P	<250	204	electrons	22.3μs integration time
Gain FPN P-P	<5	3	%	70% of saturation
RMS Read Noise	<20	14	electrons	
Leakage	<20	14.7	e-/pixel/ms	27°C
Nonlinearity	<1	1	%	
Conversion Gain	320	294	μV/e-	
Full Well Capacity	>5000	6800	electrons	
Power Dissipation	<500	350	mW	43.9Klines/sec
Lag (dark to light)	<1	0.6	%	525nm LED, 0 to 83% Sat
Lag (light to dark)	<1	0.6	%	525nm LED, 83% Sat to 0
Maximum Pixel Rate per Output	50	45	MHz	60°C
Maximum Line Rate	48.7	43.9	Klines/sec	60°C

Table 1. Comparison of ROI Design Goals and Measured Results

Table 2 shows a summary of measured results using MRDI mode, a 3.3V power supply, an oversampling ratio of 13, and a line rate of 2.7Klines/sec. The pixel output rate for all of these measurements was 80Mpixel/sec, i.e. 40Mpixel/sec per output port.

	Design Goal	Measured	Units	Notes
Offset FPN RMS	<4	0.6	electrons	316μs integration time
Offset FPN P-P	<10	11.6	electrons	316μs integration time
Gain FPN P-P	<5	3	%	70% of saturation
RMS Read Noise	<3	1.2	electrons	
Leakage	<20	42	e-/pixel/ms	35°C
Nonlinearity	<1	1	%	
Conversion Gain	320	294	μV/e-	
Full Well Capacity	>5000	6800	electrons	
Power Dissipation	<500	350	mW	2.7Klines/sec
Lag (dark to light)	<1	0.6	%	525nm LED, 0 to 83% Sat
Lag (light to dark)	<1	0.6	%	525nm LED, 83% sat to 0
Maximum Pixel Rate per Output	40	40	MHz	60°C
Maximum Line Rate	2.7	2.7	Klines/sec	60°C

Table 2. Comparison of MRDI Design Goals and Measured Results

Figure 3 shows the quantum efficiency (QE) of the sensor measured between 400nm to 1100nm. Measurements were taken every 10nm using an 8.1nm bandwidth light source. We used a $7\mu m \times 9.7\mu m$ pixel size for computing the QE. The ripples in the QE are caused by Fabry–Perot interference between the silicon nitride, silicon dioxide, and silicon interfaces.[11]

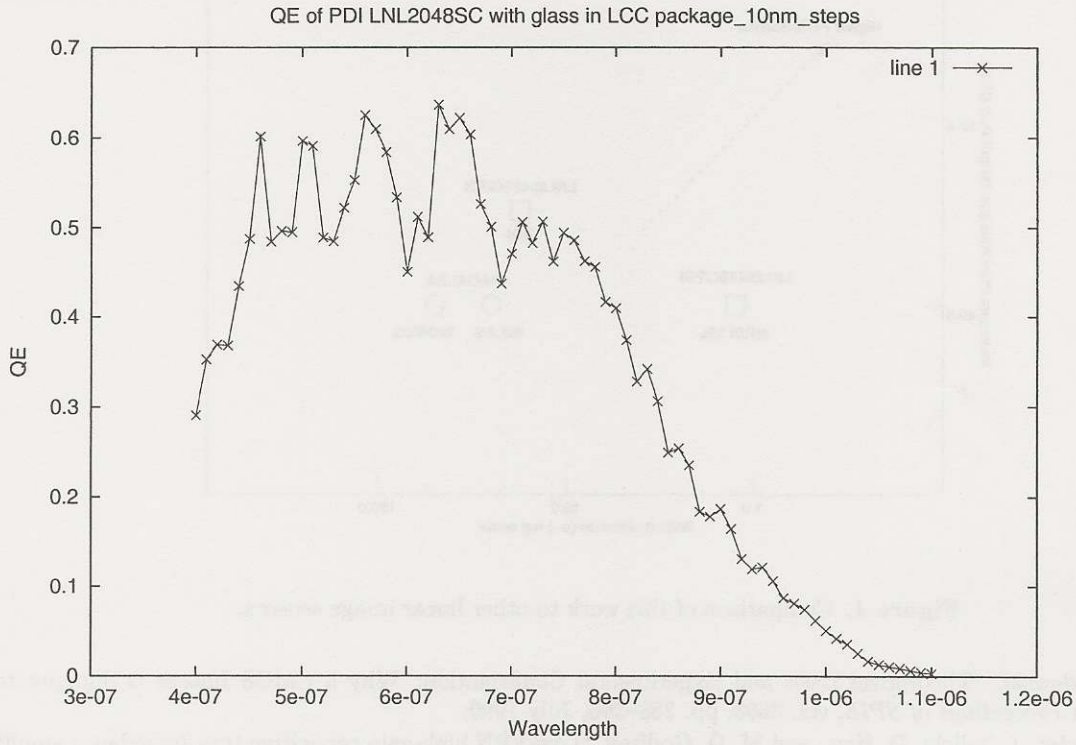

Figure 3.

4. DISCUSSION

Figure 4 shows a comparison between this work and other recently published work on high performance linear image sensors. In Figure 4 higher performance sensors are further toward the upper left, i.e. higher speed and lower read noise. The triangle shows work from R. M. Iocide et al.,[12] the circles show work from Nixon O et al.,[1] and the squares show this work. This comparison clearly shows that linear CMOS image sensors can not only out–perform linear CCDs in speed but also in read noise.

5. CONCLUSION

In this paper we have described a high speed low noise 2048×1 linear image sensor and presented measured results. This work demonstrates a linear CMOS image sensor that out–performs the best linescan CCDs available today. In the fastest read–out mode the sensor achieves 90Mpixel/sec (43.4Klines/sec), i.e. 45Mpixel/sec per output port, with 14e- RMS read noise. In the lowest noise mode with 13x oversampling of each pixel the sensor achieves 2.7Klines/sec with 1.2e- RMS read noise.

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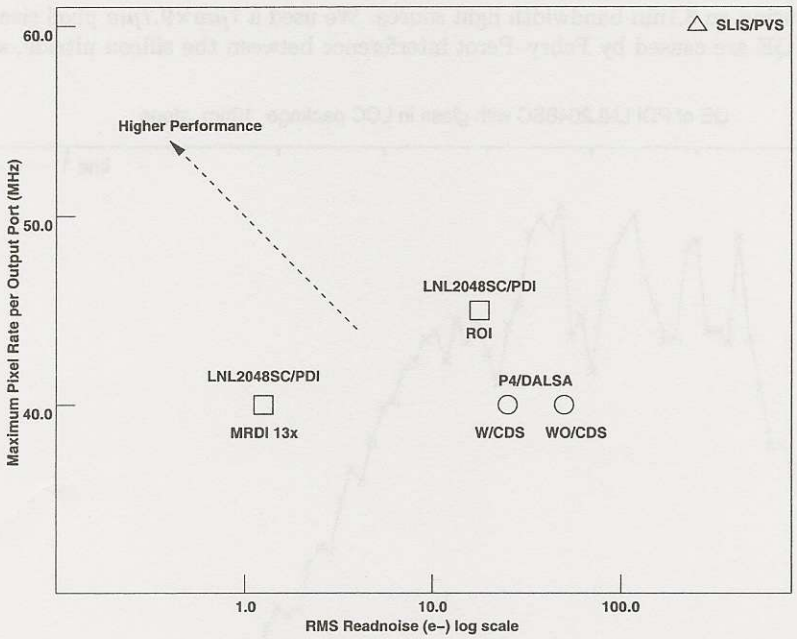

Figure 4. Comparison of this work to other linear image sensors.

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