Source follower noise limitations in CMOS active pixel sensors

K.M. Findlater, D.J. Baxter, R.K. Henderson, J.E.D. Hurwitz, L.A. Grant
STMicrolectronics Imaging Division, 33 Pinkhill, Edinburgh, EH12 7BF, UK
(Tel: +44 131 336 6000 Email: Keith.Findlater@st.com)

Introduction

Historically, the random noise performance of CMOS image sensors has been limited by the kTC (or reset) noise of the photodiode, which is not removed by double data sampling (DDS) [1]. The reset noise of the 3T APS has dominated the overall random noise in the image. Typically the random noise of such 3T sensors is not better than 30 electrons (without a severe reduction in the dynamic range). Today, more CMOS imagers are employing a pinned photodiode 4-transistor active pixel, which, when combined with correlated double sampling (CDS), eliminates the reset noise [2]. Therefore other limitations on the imager noise floor come into play. One such limitation is the noise of the pixel source-follower transistor, which contains both wide band thermal and low-frequency noise components [3]. In this paper, we discuss the extent to which this noise is limiting the random noise floor in our imagers. First, some experimental results from a test structure designed to investigate the source follower noise limitation are presented. Then a simple method for determining if the noise is 1/f or thermal noise dominated is introduced. Next, the variation in measured noise across the manufacturing processing and fabrication facilities is given.

Test structure design

The test structure (Fig. 1) is included on a revised version of a sensor presented in [4]. The first revision of the sensor exhibited a higher than expected random noise, despite the use of a pinned photodiode pixel and low-noise column parallel read-out. The test structure duplicates the source follower and access transistor configuration employed in the pixel, but with varying W/L ratio and areas for the source follower transistor. The structure provides a variety of devices with the same transconductance (and hence thermal noise) but with different size to change the 1/f component, and vice versa (Table 1). The structure is connected through the pixel array column lines to the digital read-out circuitry of the sensor and is subject to the same capacitive load as the real pixel source followers. Table 2 shows the results of the noise measurements for the structure. The readout noise of the sensor has been subtracted in quadrature from the total noise to give only the source follower compenent. The minimum device size results in a higher than desired noise, which can be attributed to the higher 1/f component. Lower transconductance values with larger area result in low source follower noise due to reduced thermal and 1/f components.

Noise measurement using variable CDS timing

As well as eliminating pixel reset noise, CDS also attenuates low frequency noise from the pixel, and the period between samples sets the low frequency cut-off of the read-out circuitry [5,6] (the high frequency cut-off can be reduced by increasing the capacitance on the bitline or reducing the driving transistor transconductance). In our test measurement, which can be performed on our test structure or on the standard pixel, the timing shown in Figure 2 can be used. When both CDS pulses are co-incident, both capacitors at the ADC input will

contain the same signal: therefore the noise signal from the source follower is eliminated. What noise remains gives a measurement of the read-out noise of the ADC. By increasing the period between the fall of CDSSIG and CDSBLK, a set of noise measurements of an imager can be produced with varying frequency components of the noise eliminated. This measurement method has the advantage that it can be implemented purely through a timing change on the sensor without any extra circuitry.

An example measurement using this method is given in Figure 3. When the 1/f component of the noise is insignificant and thermal noise dominates (such as in the larger device size) the noise measurement curve is flat over the range of CDS sample periods. Therefore this simple measurement technique can be used to show if 1/f or thermal noise limits the sensor noise floor.

Process technology measurements

Measurements of this kind have been performed on several different silicon lots and technologies to assess the contribution of the pixel source follower noise (Fig. 4). The read-out noise has been subtracted from the values in quadrature to give only the noise from the pixel. It can be seen that there is considerable variation in the source follower noise levels, both between fabs, but also within fabs. The source follower transistor size in both 0.35 micron and 0.18 micron technology was 0.8/0.35 microns. Performance does not seem to deteriorate when moving to 0.18 micron technology. We have also observed a correlation between low threshold voltage source follower transistors and lower noise. Process development is currently underway to optimise the source follower transistor noise performance.

Conclusion

In conclusion, pixel source follower noise, especially low-frequency 1/f components are becoming the limiting factor in imager noise performance. This noise source has been found to vary considerably both between technologies but also across the same nominal process. Unfortunately, the use of larger devices to reduce the 1/f component inside the pixel is not practical due to the strict constraints on pixel size. While circuit design can address the white noise by bandwidth limiting, and can attenuate low frequencies using CDS, process technology optimisation will be required to achieve very low noise pixels with small size.

References

[1] H. Tian *et. al.*, "Analysis of temporal noise in CMOS photodiode active pixel sensor", *IEEE JSSC*, vol. 36, no. 1, pp. 92-101, Jan 2001

[2] K. Yonemoto *et. al.*, "A CMOS image sensor with a simple FPN-reduction technology and a hole accumulation diode", *ISSCC Digest of Technical Papers*, pp. 102-102, Feb 2000

[3] J. Janesick, "Lux transfer: CMOS versus CCD", *Proceedings of SPIE*, vol. 4669, Jan 2002

[4] K. Findlater *et. al.*, "SXGA pinned photodiode CMOS image sensor in 0.35μm technology", *ISSCC Digest of Technical Papers*, pp. 218-219, Feb 2003

[5] Y. Degerli *et. al.*, "Analysis and reduction of signal readout circuitry temporal noise in CMOS image sensors for low-light levels", *IEEE Tran. on Electron Devices*, vol. 47, no.5, pp. 949-962, May 2000

[6] R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*, p.502, John Wiley & Sons, 1986

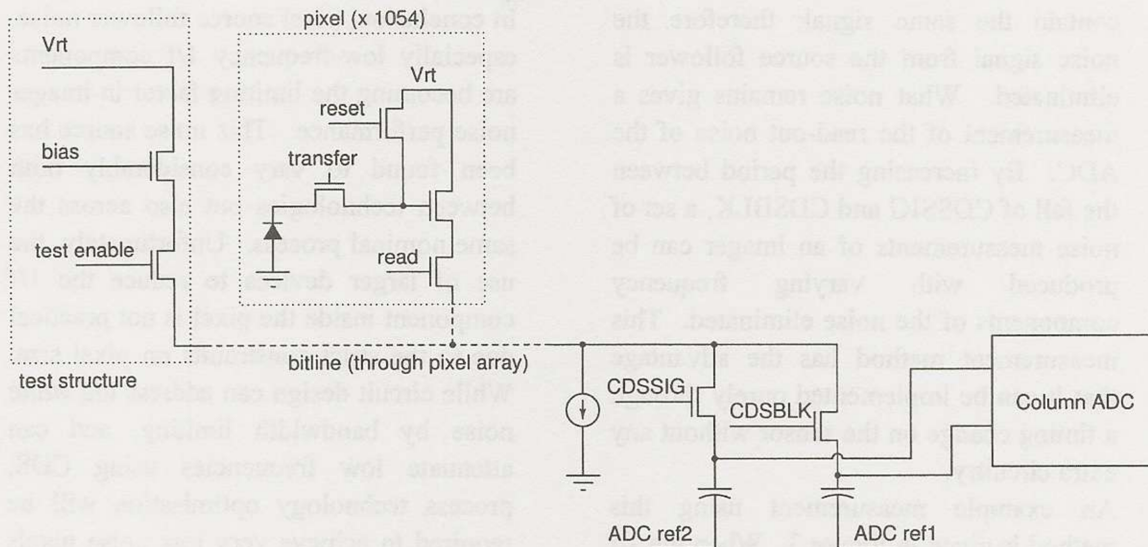

Figure 1: Schematic of source follower test structure (1 column element)

W (microns)	L (microns)	Transconductance / pixel transconductance	Area / pixel area
0.8	1.4	0.707	4
1.6	0.7		4
3.2	1.4		16
0.8	0.35	1	1
3.2	0.35	2	4

Table 1: Source follower test structure device sizes

W (μm)	L (μm)	Noise uV @ 1.2 μA	Noise uV @ 4.8 μA
0.8	0.35	173	194
0.8	1.4	88	84
1.6	0.7	100	71
3.2	0.35	154	150
3.2	1.4	150	150

Table 2: Measurements of image noise for various W, L and bias current

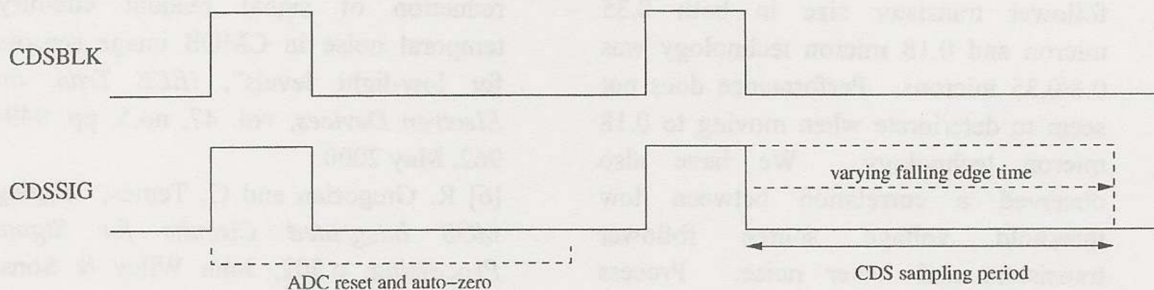

Figure 2: Measurement of source follower noise with varying CDS sample period

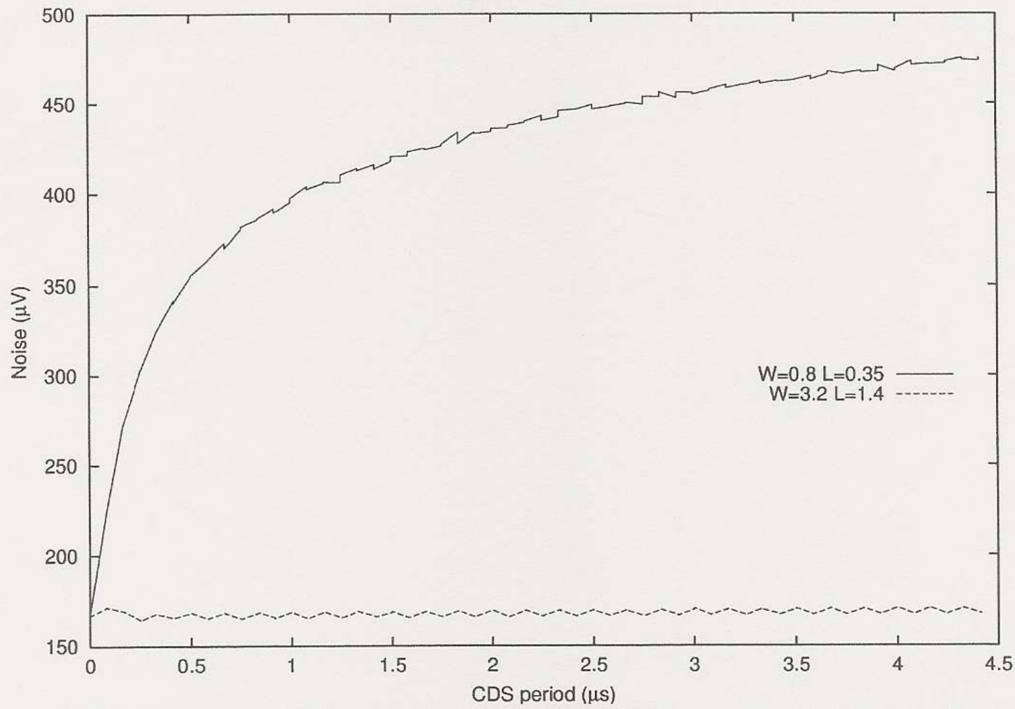

Figure 3: Measurement of source follower noise with varying CDS sample period

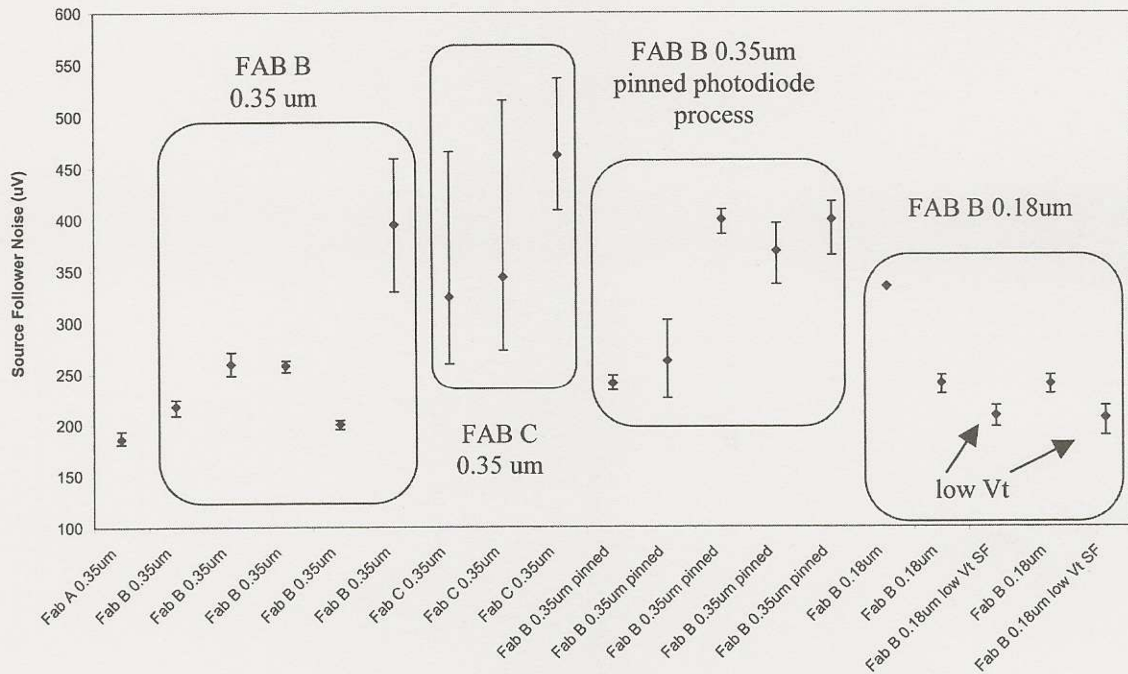

Figure 4: Source follower noise measurements for lots from various fabrication facilities.