Brain slice imaging

A 100x100 pixel CIS combining 40K frames per second and 14 bit dynamic range Tom Walschap *, Danny Scheffer *, F. Kubo ** and M. Ichikawa ***

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Abstract

The paper describes a CMOS image sensor used to monitor real time multi site neural activities. Brain slice imaging studies using voltage sensitive dyes (VSD) are suited to investigate both the functional architecture and local neural circuits. The tissue stained by VSD changes its fluorescent behavior according to its excitation, which can be measured by membrane potential. In the design of imaging sensor, large well-depth to reduce photon shot noise and high-speed readout to follow neural activities are important for this purpose, because most VSD changes its fluorescent only 0.1% by neural activities and a neuron propagate signal within one millisecond.

This paper describes the architecture and performance of the CMOS image developed. The main features are: 100x100 pixel resolution, up to 24 Me storage capacity, and a frame rate of more than 40K full frames per second. The high storage capacity ensures a dynamic range of more than 15 bit. The pixel architecture and the layout of the photodiode will be discussed in detail. The dark current of the sensor is around 21 mV/sec and has proven to be very homogenous for all pixels, allowing for straightforward correction algorithms. The sensor is designed in a 0.5 µm 2P3M CMOS technology.

1. Introduction

Brain research has been going on for a long time. There have been several sensing devices to record the movement of neurons in the brain. First systems were photodiode arrays with an external recording system based on a limited number of pixels (1980 Grinvald & Cohen). An improvement was the use of fine lithography to make connection between the photodiodes and the bond pads, not like in the previous system were they used bonding wires directly from the photodiodes to the recording structure. Conventional image sensors could not be used for VSD recording because of their current limitations

concerning the low signal to noise ratio, slow readout speed and small fill factor. A custom device can provide the brain researchers with a new recording device that has a high frame rate and low noise properties.

2. Architecture

Figure 1 shows the architecture of the image sensor. The pixel array can be driven by reset and/or row selection logic from both sides of the array. Either the logic blocks can work independently or simultaneous depending on the integration time and sensor readout mode. To reduce the row overhead time, four rows are selected simultaneously and sampled in the column sample and hold stage. The column amplifiers read out the pixel data over an on-chip multiplexer to 16 output channels. Each clock cycle, a kernel of four by four pixel is read out.

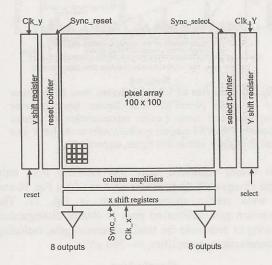


Figure 1: architecture of the image sensor

The sensor can operate in 2 different modes due to flexible sensor readout architecture. In fast readout mode, the sensor is readout only once. Off line FPN correction is necessary to remove the dark offset between pixels. In slow readout mode it is possible to readout the sensor twice during one integration time to perform off line correlated double sampling to eliminate the kTC noise and the dark offset. PRNU needs to be calibrated in both readout modes. The device is packaged in a standards JLCC 84 pins package. No special glass is used since the imaging system can take care of the optics and the necessary filters.

3. Pixel

The pixel is implemented as a classic 3-transistor active pixel using an N-well diode to the substrate as described in [1]. The pitch is 100 microns, in order to achieve acceptable charge handling performance and fill factor. The total capacitance is a contribution of the area capacitance and the perimeter capacitance of the N-well to substrate diode and the gate of the source follower in the pixel. To increase the N-well capacitance, holes are made in the N-well diode to increase the perimeter and also the total capacitance of the pixel diode. Figure 2 shows the layout of the 3-transistor pixel.

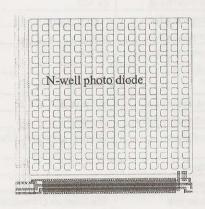


Figure 2: 3-transistor active pixel layout

The pixel pitch is $100~\mu m$, but the effective photo diode is a square of $90~\mu m$, this results in a fill factor of 80%, one of the key characteristics for optimal response for the sensor.

4. Noise source

The sensor needs a high signal to noise ratio to be able to measure changes in the signal of only 0.1%. This

means that the signal to noise ratio should be at least 10 bit including the shot noise to detect these signal variations. The dark noise is a constant noise and comes from thermal electrons and of the on-chip electronics, whereas the photon shot noise comes from the quantum effect and is proportional to the square root of the intensity. To measure small variation in the signal, the signal to noise ratio should encounter the photon shot noise. Figure 3 gives a representation of the noise sources and displays the 0.1% signal variations. It is clear that the charge handling must be larger than 10⁶ electrons to detect these variations.

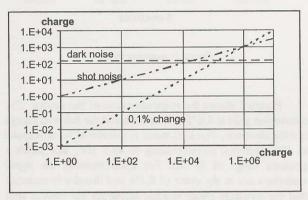


Figure 3. Different noise sources.

5. Characteristics

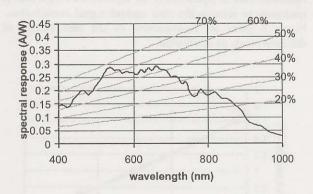


Figure 4: quantum efficiency * fill factor

Figure 4 shows the product of spectral response and fill factor as measured on a monochrome device. The peak of quantum efficiency x fill factor is 65% @ 550nm.

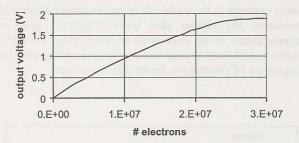


Figure 5: response curve

Figure 5 shows the response curve of the device. The conversion gain is 0,075 $\mu V/electron$ and the full well charge is 24M electrons. The kTC noise is calculated to correspond to 580 electrons, corresponding to 43.5 μV . This yields a dynamic range of 92 dB. For brain research the signal variations are in the order of 0.1% and thereby is essential that the dynamic range is high including the photon shot noise. The dynamic range including the shot noise (4900 electrons at saturation) is up to 73 dB.

The dark current of the sensor is homogeneous and only 21 mV/sec at room temperature. For short integration time of $100~\mu\text{sec}$ this results in only 2.1~mV or 28~dark current electrons. Due to repeatability, no sophisticated algorithm is necessary to remove the dark current signal contribution. Figure 6 gives the measurement of the dark current of different pixels on one device.

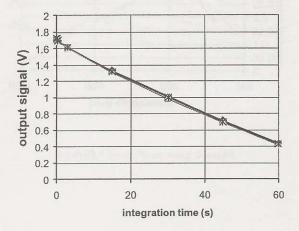


Figure 6: dark signal curve

Table1 summarizes the most important specifications of the device concerning measurements on pixel level, image quality and frame rates.

Table 1. Image sensor specifications

Pixel level	Measured results
Pixel size	100 μm x 100 μm
Spectral sensitivity	400 – 1000 nm
Spectral	Peak 0.28 A/W
Peak QE * fill factor	65% @ ?=500-650 nm
Fill factor	80% (= part of pixel without metal coverage)
MTF in x @ nyquist	0.78
@ nyquist	escapeur a la escape de
MTF in y @ nyquist	0.73
Photodiode	2.1 pF
Effective conversion	0.075 μV/e ⁻
Output voltage	1.85 V
Full well charge	24 Me
Image quality	
Temporal noise	43 μV
Dynamic range (excl. Shot noise)	41000:1 (92 dB)
S/N	4800:1 (73 dB)
Dark current	350 pA/cm ²
Dark current signal	21 mV/s
Resolution	100x100 excluding dummy rows and columns.
Others	
Pixel rate	40 Mhz
Frame rate	40k frames/s (16 outputs)
Supply Voltage	5 V
Power consumption	200 mA

Figure 7 shows a picture of the packaged device.

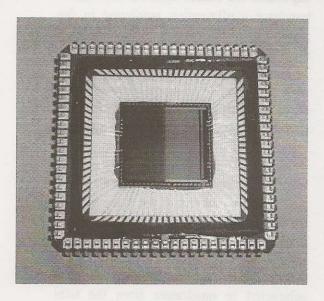


Figure 7: packaged chip

Application

The application for this device is brain slice imaging studies using voltage sensitive dyes. The tissue stained by VSD changes its fluorescent behavior according to its excitation, which can be measured by membrane potential. VSD changes its fluorescent only 0.1% by neural activities and a neuron propagate signal within one millisecond. Figure 8 represents the first experimental results of brain slice research with this image sensor.

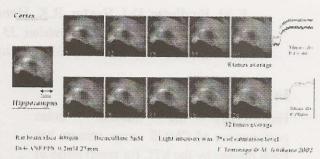


Figure 8: first test results

Conclusion

A fast low noise standard CMOS active pixel for brain research is discussed. It has 73 dB dynamic range including shot noise. The product of quantum efficiency and fill factor is 65%. It consumes 200 mA at nominal frame rate of 40k frames/s.

References

B. Dierickx, et al, "Near 100% fill factor standard CMOS active pixels", proc. 1997 CCD & AIS workshop, p. P1 (1997)