

Charge Sensitive Elements Optimised for Particle Tracking

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1. Introduction

The development of Monolithic APS (MAPS) for charged particle tracking was started at IReS-LEPSI approximately 3 years ago. The active element is a thin, moderately doped, usually of the epitaxial type, silicon layer, operated undepleted, with the front-end circuit integrated on top of it. The built-in potential, resulting from differences in doping, screens both parts and confines carriers diffusing to the electrodes. The charge collecting elements are n-well/p-epi(sub) diodes, similarly as met in some applications for visible light imaging [1]. The use of deep diodes allows a pixel with a whole area sensitive, translating to 100% of the detection efficiency. Contrary to the typical pixel detectors used in high energy physics [2], the dominating charge collection process is thermal diffusion of carriers. Classical 3T pixel designs were used at the initial phase of the development that was oriented on assessing performances for charged particle detection [3]. Operating conditions of a typical particle tracker are distinct from a typical light imager. This triggers new approaches for pixel design and new architectures of readout chips. The development is driven by requirements of vertex detectors for a future linear collider (e.g. TESLA) [4]. The paper presents two novel ideas optimising the pixel design for this application.

2. Continuous reverse polarisation

The classical 3T cell operates in a linear mode, where the charge collected is integrated and ensues voltage response of the pixel via the source follower transistor. Detectors operated in a linear mode are characterised by charge integration taking place throughout the exposition time and then the charge contents needs to be cleared to the initial state, what is achieved in the reset phase.

In visible light applications, complementary pixel architectures to the linear mode devices are pixel cells operated in a logarithmic mode. They do not integrate the charge, but a logarithmic relation approximates their response to instantaneous power of light. Logarithmic pixels provide wide dynamic range, constant image contrast and possibility of random access during all the exposition time [5,6]. The classical logarithmic pixel uses operated in weak inversion MOS transistor in diode connection as a load of charge sensitive element. The logarithmic transfer function can also be achieved using a junction diode as a load, as it is shown in Fig. 1. The load diode can be realised in a standard CMOS process by implanting a p⁺-type region into the n-well, while the

charge collecting diode remains a n-well/p-epi junction.

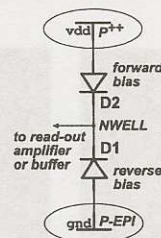


Fig. 1: Two-diode configuration providing logarithmic pixel characteristics.

Applying positive potential on the p⁺-type region, w.r.t. the substrate, provides forward bias of the junction D2, while the junction D1 is biased in a reverse direction. In darkness, the diode D2 conveys only a small value leakage current, and represents an equivalent resistance of the typical value in the T Ω order. A typical n-well/p-epi diode leakage current amounts to a few fA only, as it is shown as a function of temperature in Fig. 2.

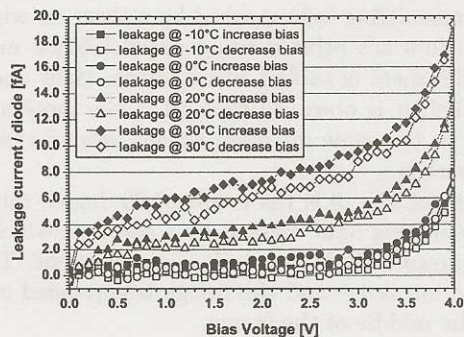


Fig. 2: Leakage current of two-diode connection as a function of temperature for a standard 0.35 μm process.

The measurements were performed on the array of 30 × 128 pixels realised in the 0.35 CMOS process, and were carried out for increasing and decreasing voltage bias. Charge collecting diodes of 4.0 × 3.7 μm² and 5.0 × 4.7 μm² were used in two halves of the array.

2.1 Application to visible light

In the first attempt the on-pixel readout circuitry was very simple, featuring a source follower placed in each pixel. The device in such a configuration was exposed to LED sources of different wavelengths. The measured

responses are shown in Fig. 3. The HLMP-4101, HLMP-CM15, HLMP-CB15 diodes were used, that are emitters of 626 nm (red), 525 nm (green) and 470 nm (blue) light, respectively. During the tests, the device was continuously illuminated with light of a varied intensity, and the pixel response was measured as the output voltage level corresponding to each illumination. The measurements of the power of the emitted light require generally calibrated photo-detectors. However, the intensity of light emitted by LED and the bias current of this element are proportional for a wide range of currents. Thus, instead of measuring directly the emitted light power, the LED current was referred to as the measure of the light intensity. The pixel responses obtained show the dynamic range of more than 5 decades of the diode current for each wavelength.

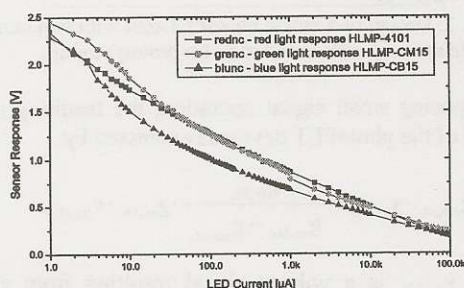


Fig. 3: Response of the two-diode logarithmic pixel to LED diode sources of different wavelengths RGB (626 nm, 524 nm, 470 nm).

2.2 Application to charged particle detection

Typical vertex detectors are effectively operated at relatively modest hit rates per pixel due to particles traversing the medium. The magnitude of the charge collected in a single case is low ($80e/h/1\mu\text{m}$ of particle track), with the voltage signal generated barely achieving a dozen or so millivolts. Under these conditions, a system allowing continuous reset can be used with the goal to cancel the leakage current effect. The reset system must provide very high equivalent resistance to allow efficient charge integration and low parasitic capacitance to preserve high charge charge-to-voltage conversion gain. Some degree of nonlinearity potentially introduced to the transfer function of the pixel response does not limit the usefulness of the continuous reset system, because of low values of the signals expected. Continuous reset opens possibility for integration of processing circuitry within area of pixel, which will be insensitive to the leakage current. Processing includes on-pixel amplifier, sampling circuitry and further extraction of signals from noise.

The pixel structure of two diodes connected in series is proposed as better adapted to the specific vertex detector environment. Its practical realisation, compatible with a standard CMOS process, is shown in Fig. 4. The current of the forward biased junction is actually limited only to the leakage current of the charge collecting diode. This is during most of the time, when there is no signal in the pixel. The level of detected signals must stay in the range for which the decay time constant, defined by the equivalent resistance of the forward biased diode and the

capacitance of the n-well, remains much longer than the detector readout time interval. This requirement is easily met in practice, where readout times in the order of 100 μs are required.

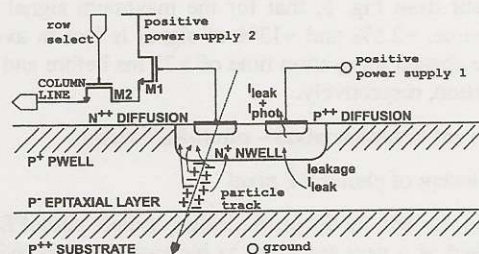


Fig. 4: Concept of the pixel structure with continuous reverse polarisation of a n-well/p-epi(sub) diode collecting generated charge.

The proposed idea was tested in one array of pixels in the MIMOSA IV prototype [7]. The pixel readout circuitry was a source follower and the row access switch transistor, connected as it is shown in Fig. 4. The tests with a high-energy particle beam resulted in similar tracking performances as were achieved with the 3T pixels. The irradiation tests with 10 keV X-rays were also performed. No degradation of particle detection efficiency was observed. The radiation-induced increase of the leakage current translates to the increased speed of the recharge after occurrence of the particle hit. The example of tests with a ^{55}Fe source, exposing the prototype to the source before and after 200 krad ionising dose, is given in Fig.5.

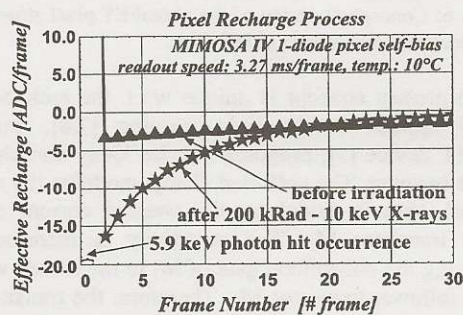


Fig. 5: Course of the recharge process of the n-well/p-epi(sub) diode before and after 200krad irradiation for the 5.9 keV photon hit occurrence at full charge collection efficiency.

Fig. 5 addresses an important issue in the use of the continuous reverse polarisation which is the recharge speed at which the n-well/p-epi diode recovers to its steady state after occurrence of the physical signal. The steady state voltage is determined by the leakage current, and the discharge time constant decreases with increasing leakage current. As a consequence, the signal could be lost if the readout was not fast enough. This risk becomes potentially more important after irradiation, when leakage currents naturally increase. Fig. 5 shows the course of the recharge process after the photon hit falling to the first

frame taken and the figure shows the resultant of many recharge processes for the case of a complete collection of $1640 e^-$ within one pixel, that corresponds to ~ 130 ADC units. The readout time of a single frame is equal to 3.27 ms (1.25 MHz readout clock frequency). It is apparent from Fig. 5, that for the maximum signal from the source, $\sim 2.5\%$ and $\sim 13\%$ of signal is lost in average for the chosen integration time of 3.27 ms before and after irradiation, respectively.

3 Current response pixel – photoFET design

3.1 Concept of photoFET pixel

The current mode pixel design, called photoFET, is proposed as a new approach to increase the sensitivity of the pixel response. Its design relies on a PMOS transistor located in a floating n-well, as it is shown in Fig 6. The design is compatible with a standard CMOS process. In its basic configuration, the photoFET element provides a built-in signal amplification capability combined with continuous reverse polarisation of the charge-collecting element and is operated at relatively high bias current in the order of a few μA . The signal amplification is achieved in charge-to-current conversion.

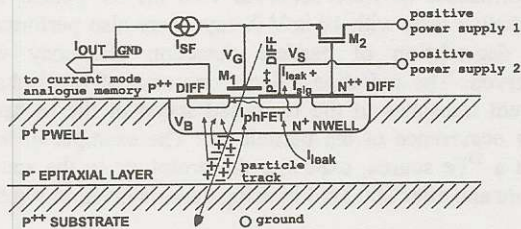


Fig. 6: Conceptual design of the photoFET pixel structure with continuous reverse polarisation.

The present concept is unique w.r.t. the architectures already applied to the light imaging [7,8], and the DEPFET device [9], proposed for the X-ray and charged particle imaging. The collected charge modifies the n-well potential, thus it modulates the channel current of the PMOS transistor M_1 . The sensitivity is increased by connecting the polysilicon gate of M_1 to the n-well via the source follower transistor M_2 . Therefore, the transistor M_1 can be driven in the high transconductance region, being controlled by the bias current of the transistor M_2 . Using the source follower, both gates, i.e. the substrate and front gates, contribute to the photoFET current response. The diode, formed by the p^+ -type source region of M_1 and the n-well, provides continuous reverse bias of the charge collecting diode. The schematic diagram of the complete pixel design based on the photoFET principle, implemented as a test structure in the prototype chip, is shown in Fig. 7. The pixel contains two memory cells, realized with transistors M_5 and M_6 , capacitors C_{s1} and C_{s2} and the related switches. The presence of memory cells enables to sample the photoFET current in two time slots for a later signal extraction in double sampling operation. The current mirror built with transistors M_3 - M_4 allow to monitor continuously current in the prototype photoFET

element. The sampled current of the current mirror was used for estimation of noise performance of the device.

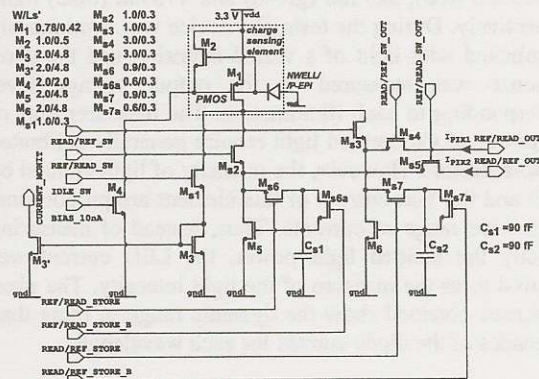


Fig. 7: Design of a single photoFET unit with two current mode memory cells as tested in the prototype chip.

Supposing small signal operation, the resulting signal current of the photoFET device is expressed by:

$$i_{out} = g_{mb,M_1} \cdot v_{bs,M_1} + \frac{g_{m,M_2}}{g_{m,M_2} + g_{mb,M_2}} \cdot g_{m,M_1} \cdot v_{bs,M_1}, \quad (1)$$

where v_{bs,M_1} is a voltage signal resulting from charge collection and $g_{m,M_1}, g_{mb,M_1}, g_{m,M_2}$ are small signal parameters of the M_1 and M_2 transistors. A linearity of the pixel response better than 0.5% for signal range $1-10^4 e^-$ was obtained by operating the PMOS transistor in strong inversion with the bias current in the order of 5-10 μA .

For some applications requiring fast and precise operation, e.g. dosimetry of radioactive sources, the integration time must be precisely defined. Under these conditions, the use of a reset transistor is unavoidable to empty the n-well from the collected charge before new integration. Fig. 4 shows possible designs of the photoFET cell, including also the traditional reset switches.

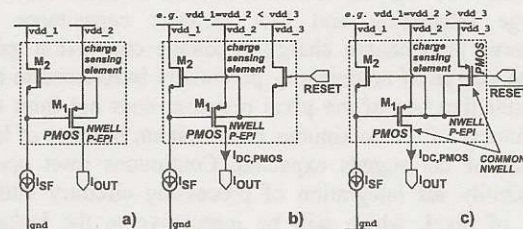


Fig. 8: Configurations of a photoFET cell; (a) continuous reverse polarisation, (b) reset using NMOS transistor, (c) reset using PMOS transistor placed in a common n-well.

3.2 Performances of photoFET pixel

The static characteristics of the photoFET cell were examined at first. Fig. 9 shows the DC current of a single photoFET PMOS transistor as a function of a source follower current and power supply voltage estimated at constant power supply and current of the source follower transistor, respectively. Good controlability of the

photoFET bias was achieved and the 5 μA current was set in the PMOS transistor for the subsequent tests.

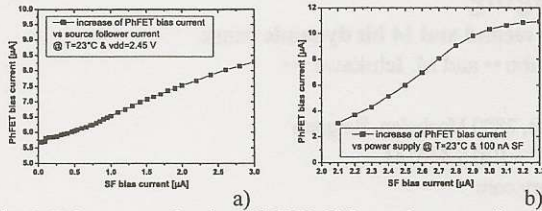


Fig. 9: DC current of a photoFET PMOS transistor as a function of (a) source follower current, (b) power supply voltage.

The basic detection performances of the photoFET device were studied with a ^{55}Fe source on a single sensor cell coupled to the chopper stabilised transresistance amplifier (not described in this text) delivering the difference between two current levels. The sample of the test results is shown in Fig. 10. The output voltage of the transresistance amplifier and the current monitor output of the photoFET, both sampled at ~ 1 ms clock interval, are shown. The measurements provided an estimate of the current response sensitivity of the photoFET cell of ~ 330 pA/e $^{-}$, for the bias current of ~ 5 μA . The noise was measured on the current monitor output below 4.5 e $^{-}$ (ENC) at room temperature for the frequency band 1 kHz - 25 MHz. The process of recovering the quiescent current level by the photoFET device lasts a few tens of ms, as it is shown in the inset of Fig.10.

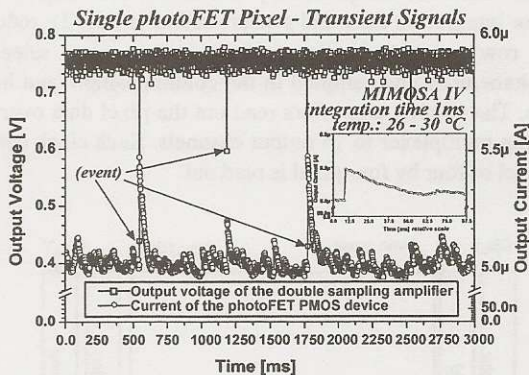


Fig. 10: Detection of 5.9 keV photons from ^{55}Fe source by a single photoFET cell. Square (transresistance amplifier) and circle (online representation of current monitor photoFET output) symbols, refer to the left Y axis and the right Y axis in this figure, respectively.

Most events registered were hits resulting from only partial charge collection, as it is apparent from Fig. 10 and the wide energy spectrum shown in Fig. 11. The conversion gain calibration peak is clearly distinguished allowing to determine the total conversion gain, including the transresistance amplifier, to ~ 200 $\mu\text{V}/e$.

Conclusions

The advantage of the pixel architecture with continuous reverse polarisation of the charge sensitive element is the elimination of the voltage drop due to the accumulation of

carriers from the leakage current. This feature allows introducing in the pixel an amplification stage. Signal amplification combined with sampling is an essential element for implementing on-line and on-chip data sparsification. As a first step towards this direction, a new pixel design, including on-pixel amplification and double sampling operation was proposed [11]. Parallel line of development, particularly appealing, because of increased sensitivity, low noise performance, easy implementation of good precision on-pixel memory cells and possibility of on-wire current summing, is current mode approach for pixel design.

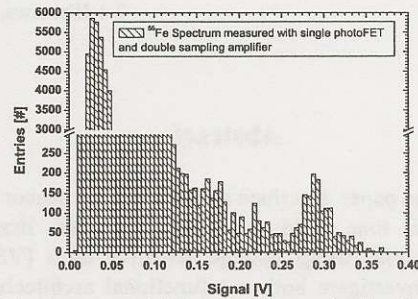


Fig. 11: Spectrum of 5.9 keV photons (calibration peak present) obtained with the single photoFET cell and the chopper transresistance amplifier in the MIMOSA IV chip.

The two-diode pixel can be used as an improved logarithmic sensor in visible light imaging, replacing topology with a diode-connected MOS transistor as the load of the charge sensitive diode.

References:

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