CMOS APS Pixel Photoresponse Prediction for Scalable CMOS Technologies

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Abstract-- **This work presents a semi-analytical diffusion-limited CMOS Active Pixel Sensor (APS) pixel photoresponse model use for maximum pixel photosignal prediction in scalable CMOS technologies.**

SUMMARY

It was recently shown [1] that for any potential pixel active area shape, a reliable estimate of the degradation of image performance is possible, so that the tradeoff between conflicting factors, such as integration photocarriers and conversion gain, could be compared per each pixel design for optimum overall sensor performance in a particular technology process. In this work, based on thorough study of the experimental data acquired from several pixel chips fabricated in two different technology processes, i.e., 0.5μm and 0.35μm CMOS processes, we extend the presented analysis and show the efficacy and the expediency of our photoresponse model in scalable CMOS processes. Moreover, we bring out clearly the possibility of a design enabling maximum output signal extraction, based on handy process and design data.

Figures 1 and 2 show two subsets of pixels of rectangular and square active area shape and decreasing photodiode dimensions fabricated in standard CMOS 0.5μm process. Figures 3 and 4 show the corresponding output curves for several wavelengths lighting. These curves share the same behavior, i.e., Fig.3 curves display a pronounced maximum response location, while in Fig.4 the curves tend to an extremum. The photoresponse model presented in [1] and summarized in table 1, enables the extraction of the unity " main area" and unity peripheral contributions to the output signal for the curves in Fig. 3 at each wavelength, and by that the identification and pixel behavior modeling (see Fig. 5). The fact that the combination of the above contributions remains invariable for all pixels at certain wavelength exposure (for a certain process) enables the extrapolation of the modeled function, and by that the revelation of the optimal photodiode geometry (for the rectangular pixels see Fig. 6).

Fig. 7 shows a subset of pixels of rectangular photodiode shape fabricated in standard CMOS 0.35μm process and designed according to the same rules as the pixels presented in Fig. 2. Note that all the pixels share a common, traditional three-transistor type readout circuitry, enabling behavior identification of different pixel types. Fig. 8 shows the corresponding measured and modeled (based on handy process and design data) output curves for several wavelengths lighting where obvious maximum response geometry is indicated. We ratify therefore that our model for photoresponse estimation of a photodiode based CMOS APS field of applicability is not constrained by a specific technology process; it can be used as a predictive tool for design optimization per each potential application in scalable CMOS technologies. Moreover, taking into consideration the general scaling tendencies we assume that the ratio between the unity "main area" and unity peripheral contributions has a slight upward trend, mostly through the reduction of mobility and life time with increasing doping levels, and shrinkage of the depletion widths. We examined the total "main area" and the total periphery contributions to the output signal separately as a function of the photodiode dimensions change. With the dimensions decrease the "main area" contribution scales down, while the periphery contribution scales up, such that their interception occurs exactly at the point where the maximum output signal is predicted by extrapolation (see Fig. 9, for the 0.5μm process). Based on the above assumption we substituted the parameters (determining the unity "main area" and unity peripheral contributions) extracted for the 0.5μm chip (at each wavelength) into the expressions for the total "main area" and the total periphery contributions in the 0.35μm design and obtained the interception exactly at the point indicated by the measurement (see Fig. 10). Note that this result is obtained for the 0.35μm CMOS design based only on the available design and process data and the parameters extracted for the 0.5μm design, i.e., there was no need in the actual 0.35μm test chip investigation, such that the optimum geometry, i.e., the pixel enabling the maximum photoresponse was predicted theoretically, based on the investigation results obtained from an older process and scaling considerations only.

REFERENCES

[1] I. Shcherback, O. Yadid-Pecht," Photoresponse analysis and pixel shape optimization for CMOS Active Pixel Sensors," *IEEE Trans. Electron Devices,* special issue on Image Sensors, Feb. 2003

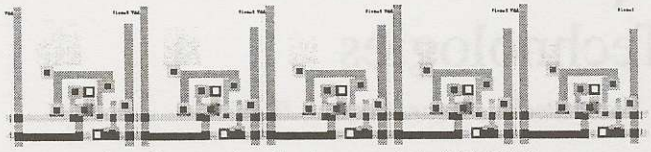

Fig. 1: A subset of square-shaped active area pixels (CMOS 0.5µm technology) with decreasing (photodiode) dimensions. The photodiode areas vary between $40\mu m^2$-$5.5\mu m^2$, and their perimeter varies between $23\mu m$ – $9.3\mu m$.

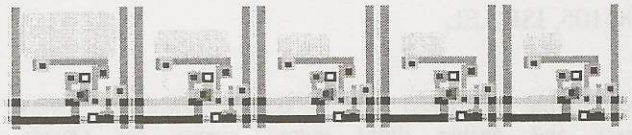

Fig. 2: A subset of rectangular-shaped active area pixels (CMOS 0.5µm technology) with decreasing (photodiode) dimensions. The photodiode areas vary between $63\mu m^2$-$13\mu m^2$, and their perimeter varies between $34\mu m$-$15.5\mu m$.

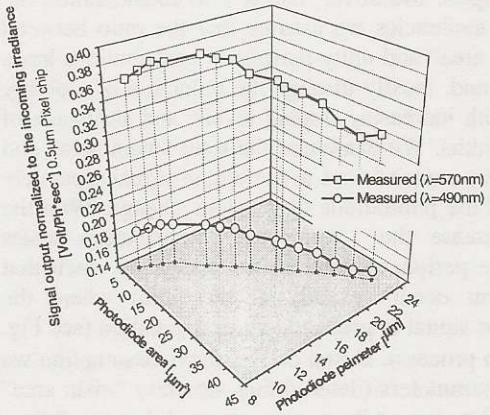

Fig. 3: Measured signal output obtained for the pixel set presented in Fig. 1, according to the photodiode linear dimensions change for two different wavelength illuminations.

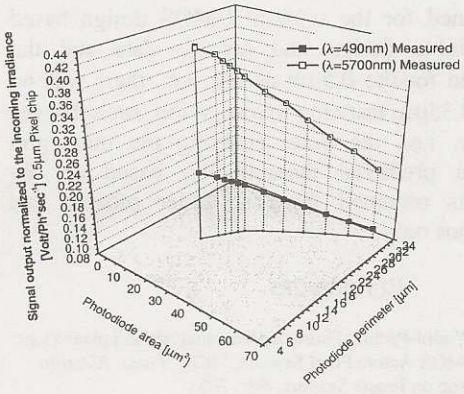

Fig. 4: Measured signal output obtained for the pixel set presented in Fig. 2, according to the photodiode linear dimensions change for two different wavelength illuminations.

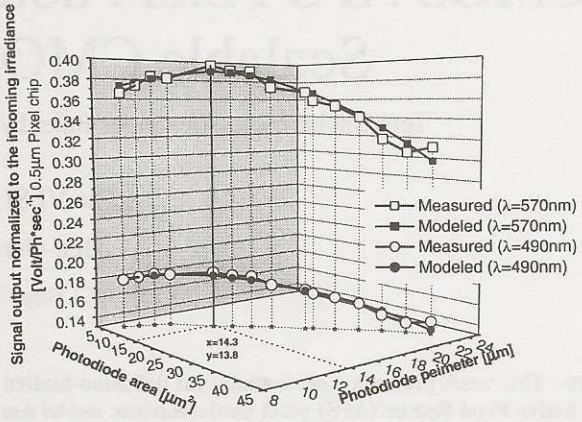

Fig. 5: A comparison of the modeled and the measured results obtained for the pixels presented in Fig. 1 for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated.

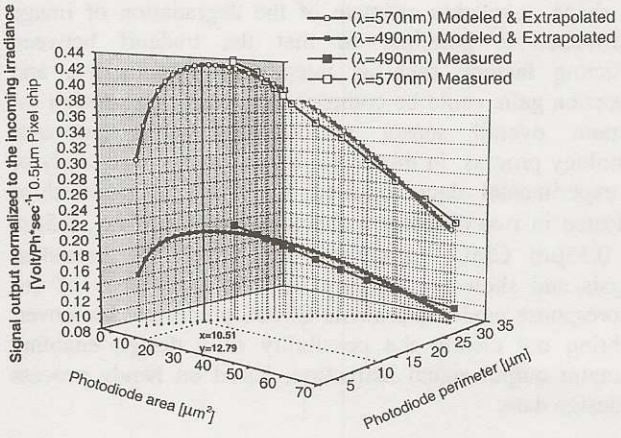

Fig. 6: A comparison of the modeled and the measured results obtained for the pixels presented in Fig. 2 for two different wavelengths. Model extrapolation points out the photodiode area and perimeter corresponding to the pixel enabling maximum photoresponse. Note that the optimal pixel was not actually designed and measured, hence the model extrapolation envisages its existence and location, i.e., its geometry dimensions.

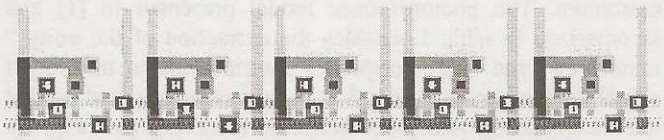

Fig. 7: A subset of rectangular-shaped active area pixels with decreasing photodiode dimensions (CMOS 0.35µm technology). The photodiode areas vary between $13.4\mu m^2$-$4.3\mu m^2$, and their perimeter varies between $15\mu m$-$8.1\mu m$.

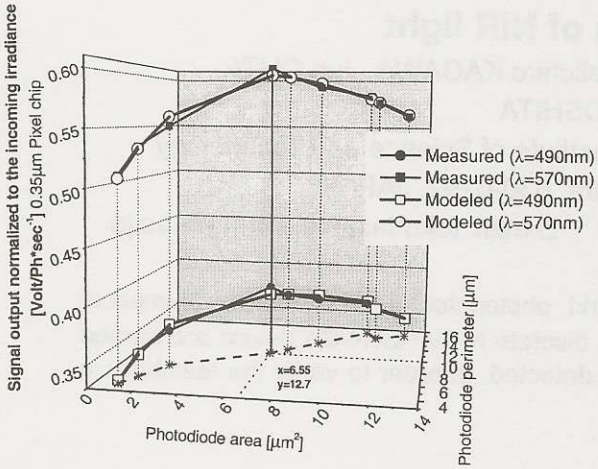

Fig. 8: A comparison of the modeled and the measured results obtained for the pixels presented in Fig. 7 for two different wavelengths. The geometry of the pixel enabling maximum photoresponse is indicated.

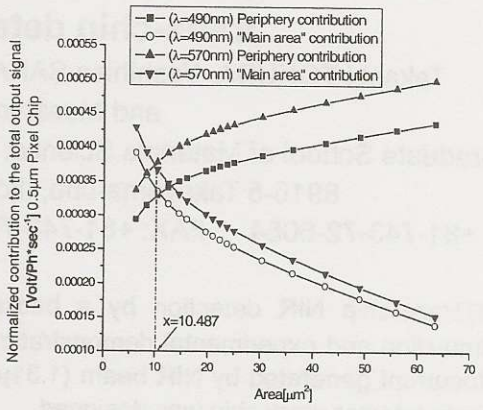

Fig. 9: Total "main area" and periphery contributions to the output signal as a function of the photodiode dimensions change for the 0.5µm CMOS pixel set presented in Fig. 2. The interception occurs exactly at the point where the maximum output signal was predicted by extrapolation in Fig. 6, thus confirming that result.

Table1: The photoresponse model

$$\frac{V_{out}(\lambda)}{N_{p\lambda}} = (\text{integration photocarriers} \times \text{conversion gain}) = \frac{k_1 A + k_2 Pd\left(\frac{S-A}{S}\right)\left(1-\frac{4Pi-P}{8L_{diff}}\right)}{k_3 A + k_4 P}$$

k_1 [μm^{-2}]	The number of electrons collected by the unity photodiode area in a time unit
k_2 [μm^{-2}]	The number of electrons collected by the unity "side-wall collecting surface" within the substrate depth
k_3 [$aF/\mu m^2$]	The bottom capacitance
k_4 [$aF/\mu m$]	The fringe capacitance
P_i [μm]	The pixel pitch
d [μm]	The depletion depth
P [μm]	The photodiode perimeter
A [μm^2]	The photodiode active area
$(S-A)$ [μm^2]	The unoccupied photodiode surroundings area within the pixel
L_{diff} [μm]	The diffusion length
$V_{out}(\lambda)$ [V]	The pixel signal output for a particular wavelength
$N_{p\lambda}$ [$Photons/\sec$]	The photon irradiance

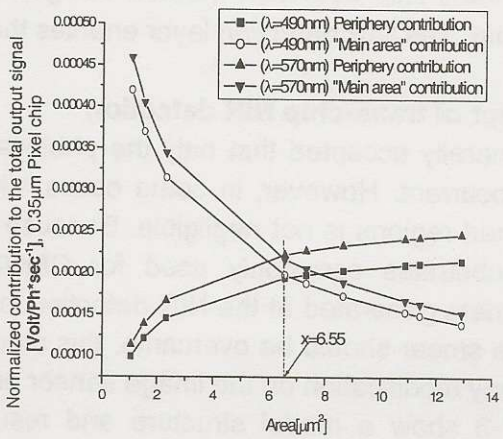

Fig. 10: Total "main area" and periphery contributions to the output signal as a function of the photodiode dimensions change for the 0.35µm CMOS pixel set presented in Fig. 7. Note that this result is obtained theoretically, based on the investigation results obtained from an older 0.5µm CMOS process and scaling considerations only. The interception occurs exactly at the point indicated by the measurement in Fig. 8, i.e., the theoretically predicted result was confirmed by the measurements.