Analysis and potentialities of backside-illuminated thinned CMOS imagers

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Abstract

The main purpose of this work is to analyse the potentialities of backside-illuminated thinned photodiode CMOS imagers, especially in terms of Quantum Efficiency, and to evaluate if the performances enhancement is strong enough to compensate the cost increase resulting from the difficult thinning post-processing out of the standard CMOS flow. Two CMOS substrate options have been considered in order to evaluate quantum efficiency, taking real doping profiles into account: lightly doped substrate (from a 0.7 µm CMOS process) and epitaxial layer on heavily doped substrate (from 0.5 µm CMOS process)

I. Introduction

CMOS imagers, now considered as a valuable alternative to CCD in many application fields, have their quantum efficiency reduced by optical filtering effects due to complex top layers structure and limited fill factor. Thinning and backside illumination (BI) have been successfully applied to CCD image sensor to improve their quantum efficiency. It can potentially be similarly applied to CMOS imagers in an attempt to allow, both the increase of impinging photons number on the photosensitive area through the suppression of top layers stack filtering, and the use of a maximal fill factor value, the whole backside surface being photosensitive. But, it has to take into account the specific features of CMOS process, mostly the limited EPI thickness in the case of the heavily doped substrate option.

II. Technological issues in backside thinned CMOS imagers

The whole process that allow to get a backside illuminated thinned imager includes several steps that have to be fulfilled :

- Substrate thinning,
- Backside accumulation,
- Antireflection coating deposition,
- Mounting and packaging.

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Several techniques can be used for each step.

First of all, due to the doping concentration generally higher for CMOS than for CCD imager, thinning process must go more deeper for CMOS. Chemical only or Chemical-Mechanical (CMP) thinning can be used. In the case of a lightly doped substrate, the control of the residual thickness is more difficult because thinning techniques usually use the concentration gradient to stop the chemical etching, resulting in a residual thickness in the range of 12 to 15 µm. For an epitaxial layer on heavily doped substrate, this substrate must be completely removed so that optical generation only takes place in the epitaxial region, otherwise the optical performances are not improved. In standard CMOS process, the epitaxial layer is usually very thin (in the range of 3 to 8 µm) but larger thickness can be obtained in some foundries.Thickness less than 5 µm can involve both breakage problems and poor quality of remaining silicon, so such processes appear as bad candidates for thinned imagers.

After the thinning process, the backside is charged positively. This creates a potential well which can capture the photoelectrons generated by short-wavelength radiation and prevents these electrons from being collected by the depletion region in the front of the device.

As illustrated in Fig.1, a bare p-type substrate will have energy bands which bend downward. To overcome this situation, it is necessary to create an electric field to drive photoelectrons to the frontside.

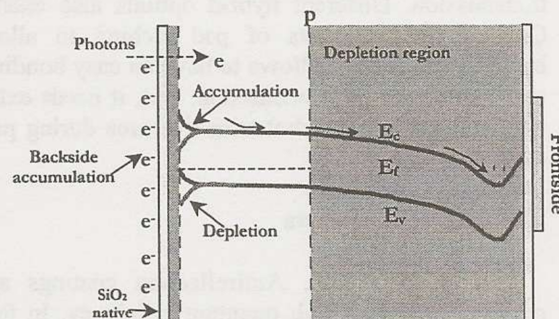

Fig. 1: Accumulation process

Most of the BI-Thinned CCDs accumulation techniques, either passive or active can be used for CMOS. The passive ones, which do not disturb the crystal lattice, involve the formation of a negatively charged thin oxide. Typical examples are the back surface charging and the flash gate in which negative charges trapped in an oxide are used to accumulate the back surface. However, it has been found that this trapped charge density can vary from the external influences and with time. The active techniques which modify the crystal lattice involve the use of ion-implantation followed by a laser annealing process to form a shallow p^+ layer. The appropriate choice of the implantation energy as well as the types of laser used for impurity activation allow to obtain a peak carrier concentration very close to the surface which reduce the width of a thin depleted layer.

A significant part of the QE enhancement for the backside illuminated imagers comes from the use of antireflection coating on the backside. Most of the BI-Thinned CCDs deposition techniques can be used for CMOS. Different antireflection coating are discussed further.

The last step is the mounting and the packaging but this is not the simplest one. Actually, because of the substrate thinness a carrier support is essential. Several mounting and packaging options are available. The simplest way is to cement the device directly against a glass support; the cement must be slightly flexible in order to relieve any thermal stresses developed due to the mismatched expansion coefficients of the silicon and glass. The accumulation and AR coating deposition must be applied before. The bonding is easy but transmission is reduced by the glass support.

Bump bonding is one of the most used technique. The bonding process consists of depositing metallic bumps on the device or the carrier support. They must be composed of materials which will form good electric connection between the two elements. This mounting system allows the best optical transmission. Different hybrid options also exists. One of them consists of pad etching to allow backside contacts. It allows to have an easy bonding and a good optical transmission. But, it needs extra masks to protect the photosensitive area during pad etching.

III. **Optical phenomena**

As for CCDs, Antireflection coatings are required to obtain high quantum efficiency. In this study, two commonly used CCD AR coating are considered and compared with a typical frontside stack of a 0.25 μm process and bare silicon. As shown in Fig. 2, transmission is limited by silicon reflectivity.

The use of HfO_2 allows the increase of small wavelengths optical transmission. The addition of MgF_2 increases the long wavelengths transmission and an homogeneous transmission over a large spectral domain can be obtained.

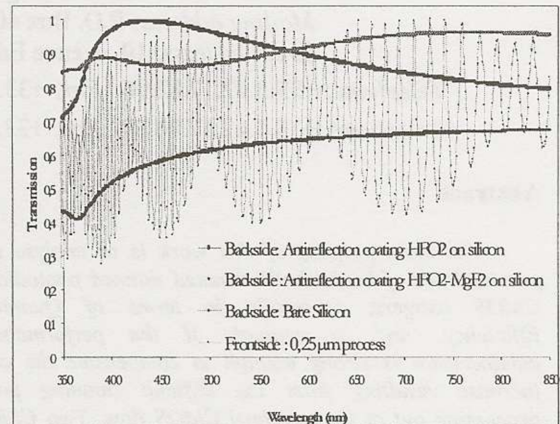

Fig. 2: Transmission of two antireflection coatings

As the silicon thickness becomes smaller, interference phenomenon, the fringing, appears (Fig.3) for long wavelengths that will degrade the quantum efficiency. Actually, reflections between the nearly parallel front and back surfaces leads to unwanted fringes of constructive and destructive interference which artificially modulate the transmission.

Antireflection coatings also helps to reduce fringing.

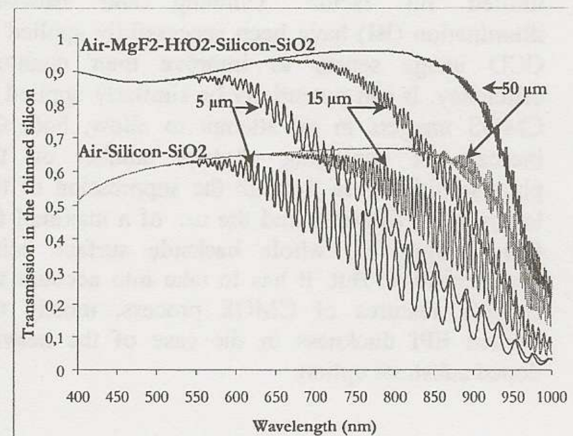

Fig. 3: Thickness influence on the fringing phenomenon

This demonstrates that using a too thin substrate will not allow to improve the optical performances.

IV. Quantum efficiency

Internal quantum efficiency has been determined for the two types of substrates. An analytical model has firstly been developed that takes the accumulation area into account and the surface recombination velocity; then, physical simulations have been performed.

As shown in Fig. 4, the description of the evaluated structure depends on the type of CMOS substrate. For both types, the depletion region is less extended

for CMOS and more distant from the backside surface than for CCDs. On that account, the direct collection by the depletion region has a weak influence on the quantum efficiency.

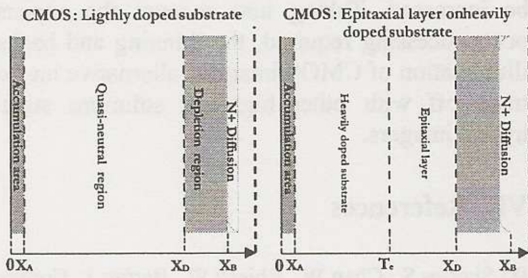

Fig. 4: Backside illuminated thinned imagers cross sections

As we consider that, for the epitaxial layer on heavily doped substrate, the EPI is reached during the thinning process, the variation of thickness is interpreted as the variation of the epitaxial layer which implies that the EPI thickness is adjustable (not always easily available from standard foundries).

The same devices has been simulated with physical 2D simulations (ISE-TCAD environment). The simulated structure is shown on the Fig.7.

As for the analytical model, a backside ion-implantation is considered. The same parameters for surface recombination velocity and the power supply are used. The Epitaxial layer on heavily doped substrate profile for a thickness of 6 µm is from an existing 0.5 µm process, the others are extrapolated from this one in order to obtain a larger epitaxial layer.

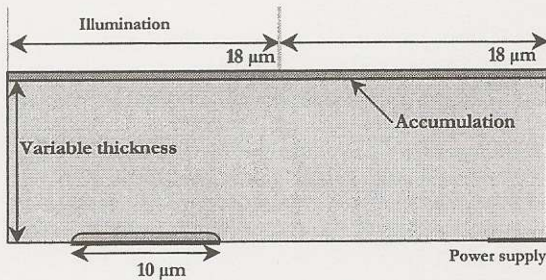

Fig. 5: Structure simulated with ISE-TCAD

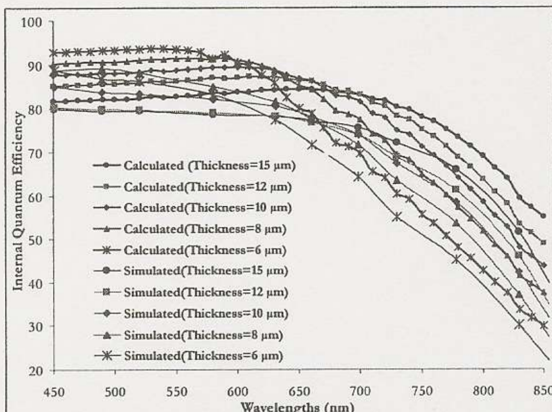

Fig. 6: Thickness influence on the internal QE of a lightly doped substrate BI imager from analytical modeling and simulations

Figures 6 and 7 provide the results of calculations and simulations for the two substrate types. By comparing these results, it can be seen that the internal quantum efficiency determined for the two types of CMOS substrates are fairly similar. One can notice that poor results are obtained for thickness of about 6 µm (current value for standard EPI on highly doped substrate process)
Good candidate for thinned imagers appear to have thickness in the range of 10 to 12 µm.

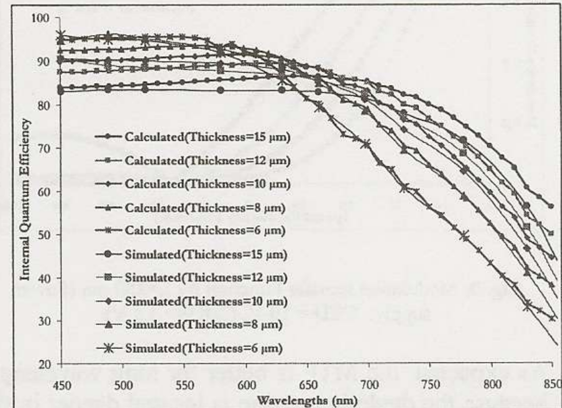

Fig. 7: Thickness influence on the internal QE of an epitaxial layer on a heavily doped substrate BI imager from analytical modeling and simulations

By combining transmission (using AR coating) and internal quantum efficiency, the external QE curve can be obtained. Results are given in figure 8 with the thickness as a parameter : the quantum efficiency is fairly enhanced and can be in the range of 75- 80% over a wide spectral domain (400-750nm) for thickness of 15µm. The epi on heavily doped substrate (EPI) technologies provide good results in the visible domain if the thickness is larger than 10 µm. For that range of thickness, it allow to get better results than for a lightly doped substrate.

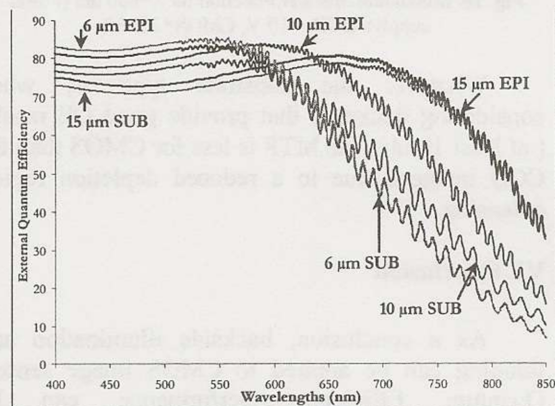

Fig. 8: Thickness influence on the External QE for the two types of substrates

V. Modulation transfer Function

The modulation transfer function of back illuminated photodiodes have also been calculated for two wavelengths (Fig.9 et 10) and are compared with similar CCD structures (same size and same number of pixel).

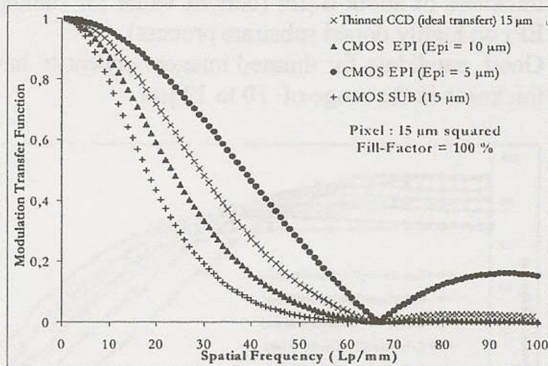

Fig. 9: Modulation transfer Function for λ=350 nm (Power supply: CCD = 10 V, CMOS= 3.3 V)

As expected, the MTF is better for long wavelength because the depletion region is located deeper in the substrate than for frontside devices.

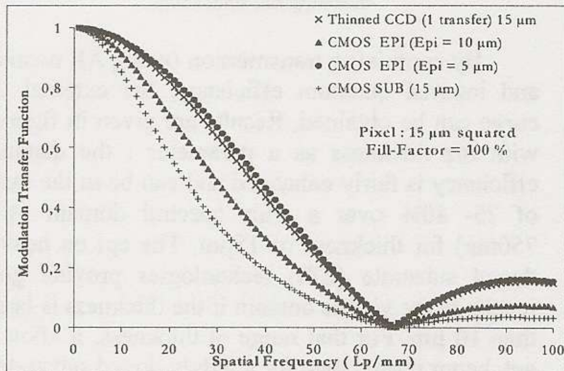

Fig. 10: Modulation transfer Function for λ=850 nm (Power supply: CCD = 10 V, CMOS= 3.3 V)

Whatever the substrate type is, when considering thickness that provide good QE results (at least 10µm), the MTF is less for CMOS than for CCD imagers, due to a reduced depletion region extension.

VI. Conclusion

As a conclusion, backside illumination and thinning can be applied to CMOS image sensor: Quantum Efficiency performance can be significantly enhanced when compared to frontside illumination, but due to limited voltage range used, the good QE performances are mostly restricted to the visible domain. The enhancement of the performances is significant but a thinned standard CMOS image sensor will not reach the best BI CCD level in terms of quantum efficiency and modulation transfer function. Furthermore, this improvement may in some case not be obtained from standard CMOS process if EPI thickness is too thin or cannot be increased. Taking into account the expensive post-processing required, the thinning and backside illumination of CMOS imagers alternative has to be trade off with other high-end solutions such as hybrid imagers.

VII. References

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