Design Consideration of FPN suppression circuit for a 1.25″ 8.3M-pixel digital output CMOS APS

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Abstract

Fixed pattern noise (FPN) in a 1.25-inch CMOS active pixel sensor (APS) developed for compact ultrahigh-definition cameras has been analyzed. And a suppression circuit has been designed for column FPN, the most dominant form of FPN and the most visually disturbing in this sensor. The column FPN suppression circuit consists of a part of extracting column FPN data and a part of subtracting it from sensor output. When extracting column FPN data, averaging is required to minimize the effects of random noise and the pixel-random FPN component. The results of testing an experimental circuit revealed that column FPN could be reduced to less than 1 LSB in terms of a peak-to-peak value when using column FPN data obtained by performing averaging over 22 rows and 32 frames or more.

Introduction

The development of practical ultrahigh-definition video systems is eagerly awaited by a wide variety of fields including broadcasting, movie production, health care, and education. With this background, we have been researching an ultra-high definition, wide screen image system that can provide viewers with a sensation of reality for next-generation broadcast services [1],[2]. In particular, our targets are cameras and image sensors for use in an ultrahigh-definition video system as a promising candidate for such broadcasting [3]. In recent research, we have focused our design efforts on a 1.25-inch system for reducing camera size and have developed a 1.25-inch CMOS active pixel sensor (APS) [4]. This CMOS sensor employs a column-parallel structure to deal with the high data rate which are necessary for ultrahigh-definition motion picture. The problem here, however, is that vertical-stripe shaped fixed pattern noise (FPN) originating in this parallel-columns structure is generated. This type of FPN must be suppressed in order for cameras that use this sensor to achieve high picture quality. For this reason, we have analyzed FPN in the above image sensor and have used the results of analysis to design an FPN suppression circuit.

Image Sensor and Noise Characteristics

Table 1: Sensor specifications

Optical Format	1.25″
Resolution	3840(H)×2160(V)
Pixel Size	4.2μm square
Frame Rate	60 Hz
	progressive
Output	10 bit
	16 parallel

The image sensor features 3840×2160 effective pixels (3936×2196 total pixels), a pixel size of 4.2-μm square, a 60-fps progressive scanning, and 10-bit 16-parallel digital output (Table 1). As mentioned above, this sensor employs a parallel-columns structure to deal with the high data rates. Here, pixel output is first processed by analog gain amplifiers provided for every column and by analog-to-digital converters (ADC) provided for every two columns, and is then stored temporarily in SRAM before being read out progressively. To achieve a pixel pitch of 4.2 μm the analog gain amplifiers are positioned above and below the pixel array, one for each column, and the ADCs are likewise positioned above and below the pixel array with

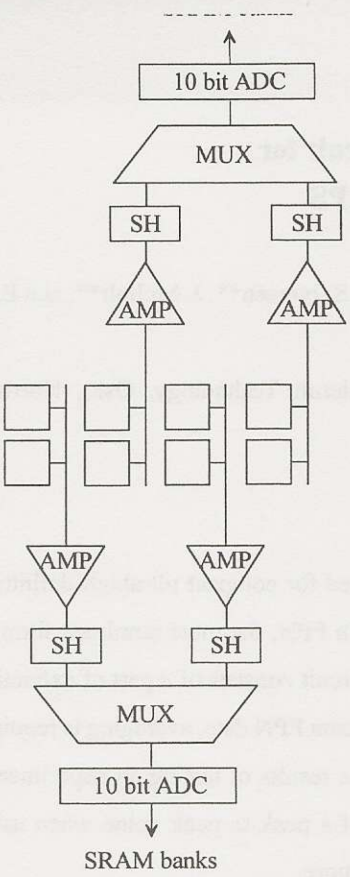


Figure 1: Signal path from pixel to ADC.

two columns sharing the same ADC by appropriate timing (Fig. 1). This structure gives rise to vertical-stripe shaped FPN caused by nonuniform characteristics in the analog-gain amplifiers and ADCs. In addition, the combination of analog-gain amplifiers and ADCs in this way is supposed to produce a 4-column cyclic pattern within the vertical-stripe FPN.

We measured each FPN component under dark conditions. First, we determined each FPN component from the value obtained by summing pixel values and taking their average of 32 frames to eliminate the effects of random noise (RN). We then measured the FPN component in the horizontal direction (column-random FPN) by summing values over 100 pixels in the row direction and taking their average, and measured the FPN component in the vertical direction (row-random FPN) by summing values over 100 pixels in the column direction and taking their average. In addition, the two-dimensional random FPN component (pixel-random FPN) is the value obtained by subtracting the column-random component and row-random component from the total FPN. On the other hand, RN was measured by subtracting the determined FPN from the original video signal. These measured values are expressed in the form of root-mean-square least significant bit [rms- LSB]. In this 10-bit digital output sensor, 1 LSB at the output port of the sensor is equivalent 16 e^- at pixel. Measurement results (Table 2) revealed that random noise is 2.46 [rms-LSB] and that FPN is 1.38 [rms-LSB], and furthermore that the FPN component occurring every column is the largest of all FPN components. Since column FPN is the most visible disturbance, we investigated a suppression circuit for that type of FPN.

Table 2: Characteristics of sensor noise

Noise	Value [rms LSB]
RN	**2.46**
FPN	**1.38**
Pixel Random	0.75
Row Random	0.12
Column Random	**1.15**
4 Column Cycle	0.65
Otherwise	0.95

Column FPN extraction

To suppress FPN under dark conditions, it must first be extracted and then subtracted from the signal. In particular, to extract our targeted column FPN with good accuracy, RN and the other FPN components must be sufficiently suppressed. Here, we have set the goal for suppression of RN and the other FPN components to be "$6\sigma < 1$ LSB" in accordance with the typical conversion from peak-to-peak value to rms value. σ, standard deviation, is assumed to be equivalent to rms value in Poisson distribution is assumed. Based on the results of Table 2, we see that output signals must be subjected to averaging 20 times at least in row direction so that pixel-random FPN satisfies this condition. Table 2 also indicated that averaging time must be 218 at least in row and/or frame direction so that RN satisfies the condition.

A self-calibration functionality is incorporated in each ADC cell of the sensor to compensate ADC's input-offset voltage nonuniformity. When this function is activating, ADC offset voltages per frame and per row are taken in by the sensor during the vertical blanking period and are subtracted from signals in the digital domain. These offset signals, however, do not satisfy the condition that the effects of random-noise and the pixel-random FPN component be sufficiently minimized. We instead decided to use external memory to save extracted column FPN data and an external circuit to perform subtraction. Based on the above, we set out to design a circuit.

Circuit Design

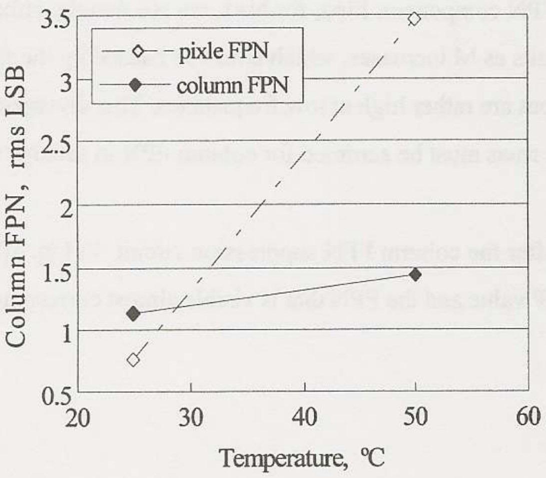
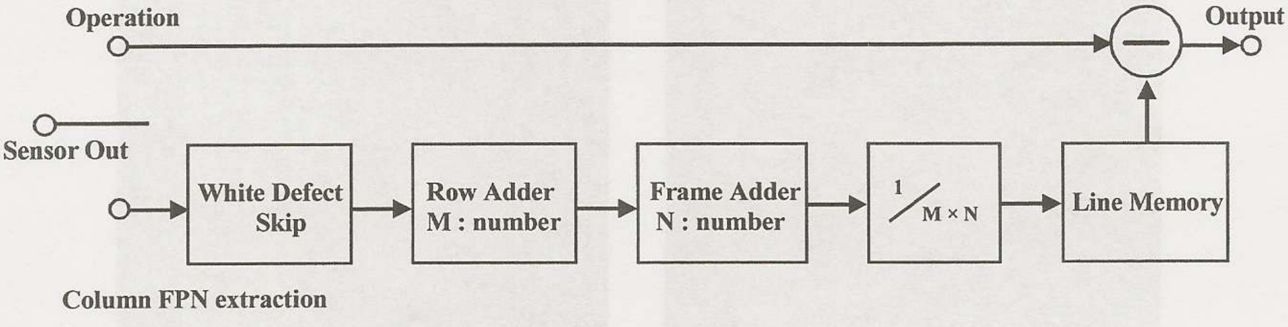


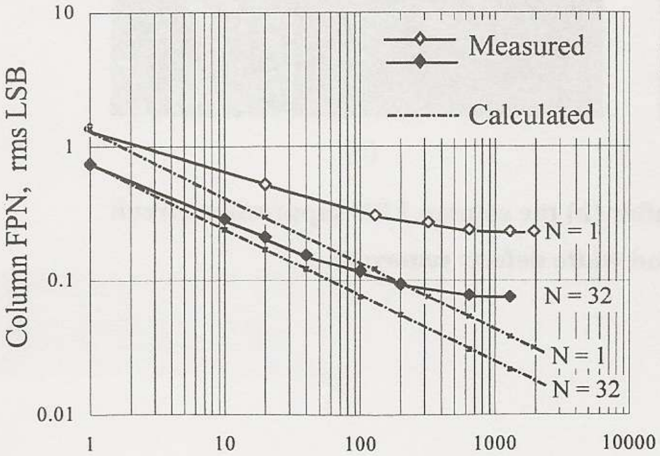
Figure 2: FPN temperature characteristic.

We began by measuring the temperature dependency of column FPN in order to determine whether column FPN data should be updated during camera operation (Fig. 2). It was found that although column FPN increases with increasing of temperature, it is gradually being less than 0.3 [rms-LSB] with increasing of temperature of about 25ºC. In fact, the pixel-random FPN component comes to dominate as sensor temperature rises, and while some countermeasure is needed in this regard, the minimal effects of temperature on column FPN means that "real-time FPN updating" is not necessarily required. In this way, even effective pixels can be used as the target for computing data to extract FPN. Column FPN also includes 4-column cyclic noise as shown in Table 2, and while this noise is not processed in this experimental circuit, extracting it in a separate process would save on memory.

Figure 3 shows a block diagram of the designed circuit. When extracting column FPN data, "sensor out" connects to the column-FPN-extraction circuit. This circuit first compares the output level of each pixel with a set level in the skip circuit, and treats high output as white defects to be excluded from calculations. It then performs calculations for the number of rows set for each frame and repeats that calculation for the number of frames set. Next, the circuit divides the current result by the total number of calculations and saves that result in external memory. The system subtracts column FPN data in memory from "sensor out" to output signals with column FPN suppressed during camera operation. The external memory used here is a line memory whose number of pixels equals to the number of horizontal pixels in the sensor.



PN suppression circuit.



Measurement Results

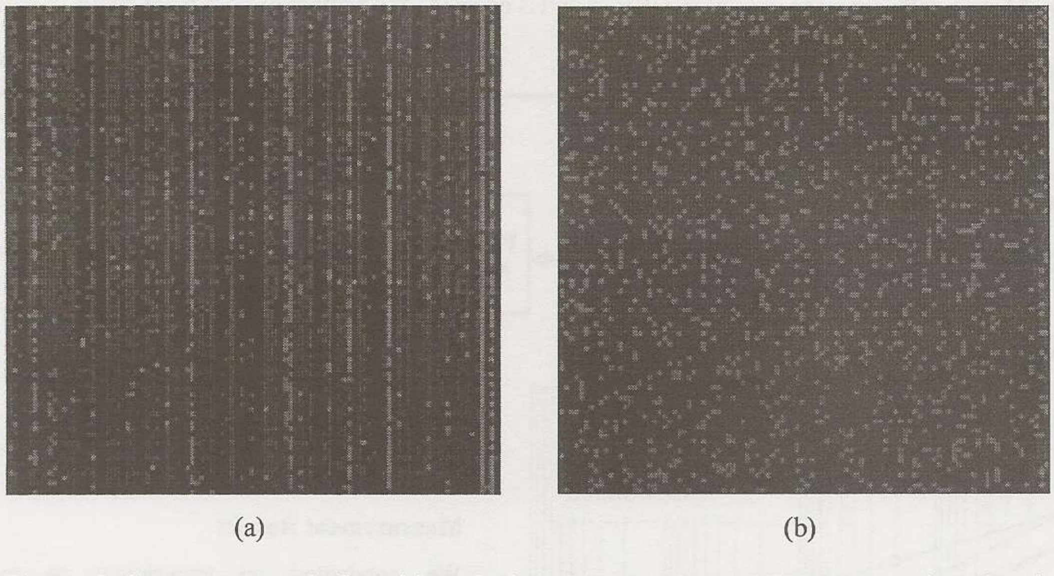
We conducted an experiment to examine the effectiveness of using this column FPN suppression circuit in sensor output. In the experiment, we measured remained column FPN included in the output signal after suppression while varying the number of rows M and the number of frames N used in calculating and extracting column FPN data. Figure 4 shows measured and calculated results. Here, when calculating remained column FPN components in the output picture, averaging was performed 100 times in the row direction. It must be noted that the number of averaging sets a limit to the accuracy of the measurement. The limit is determined by the remained pixel-random FPN component after averaging. It is calculated that the limit is 0.075 [rms-LSB] corresponding to $1/\sqrt{100}$ of the pixel-random FPN component. First, for N=1, we see that the effects of column FPN suppression diverge somewhat from calculated results as M increases, which could be caused by the fact that the frequency characteristics of random noise are not uniform but are rather high at low frequencies. This divergence can be prevented by increasing N. For N=32, we see that at least 22 rows must be summed for column FPN to satisfy “$6\sigma < 1$ LSB.”

Figure 5 shows the center of a 100 × 100-pixel image before and after the column FPN suppression circuit. In Fig. 5(b), column FPN has been suppressed to less than 1 LSB in terms of a PP value and the FPN that is visible almost corresponds to the pixel-random FPN component.

Figure 4: Remained column FPN after the column FPN suppression circuit.

Conclusions

In this paper, we analyzed column FPN in a 1.25-inch 8.3M-pixel digital output CMOS APS developed for ultrahigh-definition video systems, and designed a suppression circuit for that FPN. It was found that we should incorporate a column FPN suppression circuit into a camera so that FPN could be extracted and stored and then subtracted from sensor output signal. It was shown, in particular, that column FPN data extracted by averaging over 22 rows and 32 frames or more could suppress column FPN to less than 1 LSB in terms of a PP value without being affected by random noise and the pixel-random FPN component. The next dominant FPN is pixel-random FPN after column FPN has been suppressed, and we intend to study the suppression of it in future research.



(a) (b)

Figure 5: Sensor output before (a) and after (b) the column FPN suppression circuit (×16 increased gain and white defects removed).

References

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