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Process and Pixels for High Performance Imager in SOI-CMOS Technology

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Abstract

We present architecture, process design and results from test pixels of Active Pixel Sensor (APS) imagers implemented in SOI-CMOS technology. Fabricated test devices have digital control and analog readout circuits implemented in a partially-depleted 0.8μm SOI process. The conventional SOI process has been altered by adding steps for etching the buried oxide and two additional implants to enable photodiodes to be fabricated in the low-doped, otherwise unused, handle wafer. Results on *front illuminated* photodiode arrays indicate that peak Quantum Efficiency (QE) >70%, increasing to 90% under Lambertian illumination, can be achieved with 2-10x improvement in peak and red spectral response, respectively, compared to bulk APS imagers. This dramatic improvement is the result of large (~16 um) depletion widths in the low-doped handle wafer. Dark current tests on photodiodes and pixels indicate a periphery-dominated, voltage-dependent, leakage current of 1-20 nA/cm^2 over the range of 0-3V. Pixel linearity error of ~4% is observed at 80% of saturation. Test results indicate directions for further improvement in the implant placement and doping for reduction of the dark current.

Introduction

Spectacular progress has been made in making large format imagers using bulk-CMOS foundries by altering the conventional CMOS process flow to integrate a CMOS imager front-end with high performance processors. However, several major challenges remain. These include obtaining pixels with low and anomaly-free dark-current, low cross-talk, high linearity, good response uniformity and high dynamic range. Non-planarity in the junction area, resulting from LOCOS or STI isolation, high doping, and high electric fields cause problems for dark current reduction. Simultaneously optimizing for small depletion widths for deep sub-micron FETs and large depletion widths around the photodiode junction causes problems with cross-talk and quantum efficiency. These limitations prevent APS imagers from achieving the high performance of their CCD counterparts.

Attempts have been made to improve on the diode dark current characteristics using buried diodes.[1] However, there has also been a strong desire to integrate pixels with CCD-like response with CMOS circuit capabilities. Some have attempted to bridge the gap by fabricating CCDs in an SOI process, resulting in a less than ideal combination of technologies that does not take full advantage of the lower voltage and random access aspects of the APS concept.[2,3]

Despite its significant advantages for high-speed (RF), high-density VLSI, presence on the SIA roadmap and recent maturity, SOI-CMOS is not generally considered for imaging.[4,5] A primary reason is that photodiodes and pixels fabricated in the thin (50-200 nm) active region containing the SOI-FETs (Figure 1a) will have poor optical response. This "outside the buried oxide (BOX)" thinking has not proved successful despite many attempts to improve their performance.[6] Other areas of concern, including the integrity of the pixel photodiode, MOS transistor leakage current, the ability to fabricate mixed signal circuits, reliability and cost have all been successfully dealt with in the development of bulk APS imagers.

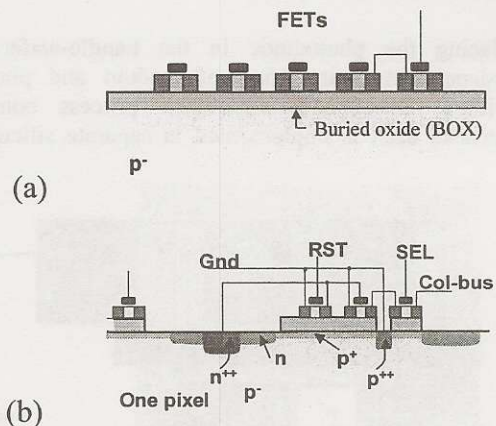

Figure 1: The conventional SOI-CMOS cross-section (a) has been modified for more optimal photoresponse by (b) placing the photodiode in the handle-wafer. Implants in the pixel diode structure minimize surface effects on dark rate.

Initial attempts to use the handle wafer of an SOI device as an active part of the light collection process used a transistor collecting region.[7] However, more successful results were achieved for particle.[8] and photodetectors[9,10] by implementing diode detectors in the handle-wafer by etching the BOX and placing the diode inside the BOX cut, as shown in Figure 1b. The handle-wafer diode is connected to the MOSFETs in the SOI-layer during metallization.

We have previously reported on improved photoresponse from SOI-based photodiodes using this "inside-the-BOX" approach.[11] Subsequently, others have reported on a similar structure, but with low quantum efficiency and large dark current.[12] In this paper, we present the design and process optimization to improve both QE and dark current. In order to verify efficacy of the design and process techniques, several different types of pixels with different implant placements and diode area and perimeters have been implemented. We report the imaging characteristics of these pixels.

Design

Small arrays of both photodiodes and test-pixels were implemented using a 0.8 μm partially-depleted SOI-CMOS process (3.3V V_{dd}). Each test pixel array consists of a conventional "3-T" pixel: a photodiode (with attached reset FET) buffered by an n-channel source-follower and an output select switch. Handle wafers fabricated using a smart-cut process were low doped ($\sim 5\times10^{12}/cm^3$). The handle wafer is created in the smart-cut process by bonding two thermally grown oxide surfaces (which form the BOX), preserving both oxide and $Si\text{-}SiO_2$ interface quality, critical for obtaining low dark currents in the pixels.

Placing the photodiode in the handle-wafer enables independent optimization of readout and photodiodes without introducing significant process complexities because each is implemented in separate silicon layers.

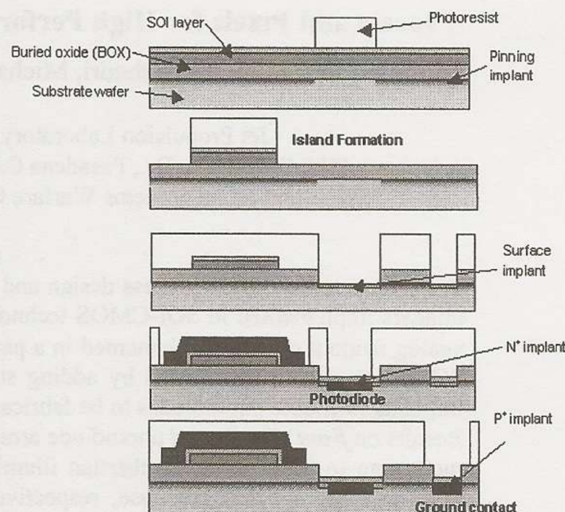

Figure 2: Key steps for incorporating the photodiode into the SOI process flow.

This allows imager designs with low handle-wafer doping for excellent photo-response and low cross-talk. However, high-quality photodiodes require process optimization of two additional implants, as shown in fig. 1b. These are: (i) Pinning implant (PI): a p-implant under the BOX, and (ii) Surface-passivation implant (SI): a n or p implant in the BOX-cut area. These implants hold the $Si\text{-}SiO_2$ interface in equilibrium to eliminate interface-related dark current generation. The surface implant also prevents a tunneling between heavily-doped areas, and reduces the surface electric field.

The primary goals of our test matrix designs were to determine achievable QE improvement based on the earlier results, as well as to explore the level and area/periphery dependences of dark current in the BOX photodiodes as a function of SI and PI implant profile. Our designs, therefore, varied pixel pitch (10, 15, 20, & 28.6 μm) and BOX cut width (7, 10 & 13 um) and

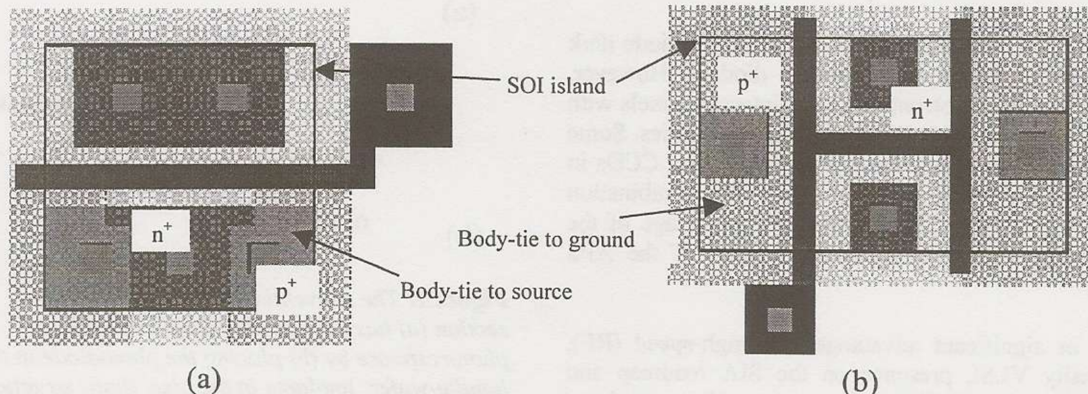

Figure 3: In-pixel FETs incorporated into the design had body ties to either (a) source, or (b) directly to ground.

shape. Two different body-tie methods were also explored to eliminate floating-body effects in the partially depleted in-pixel SOI FETs (see Figure 3).

The modified SOI process flow to implement the test matrix is shown in Figure 2. The pinning implant (boron) is carried out first through the BOX, except in areas where there will be BOX-cuts. Following the SOI island formation, the BOX layer is etched, and the surface implant (phosphorus) is applied. After this, the process-flow is the same as that of a conventional SOI, except that the BOX-cut area receives appropriate n^+ and p^+ implant during subsequent S/D implants.

Results and discussion

Figure 4 shows the measured spectral QE of a *front-illuminated* baseline photodiode. A peak QE of 90% is observed for a Lambertian source and >70% for near-normal incidence in the far field. These results correspond to an increase of ~2x at the peak and ~10x in the NIR above that expected for a typical *front illuminated* APS imager fabricated using bulk technology, and is comparable to or better than back-illuminated CCDs.

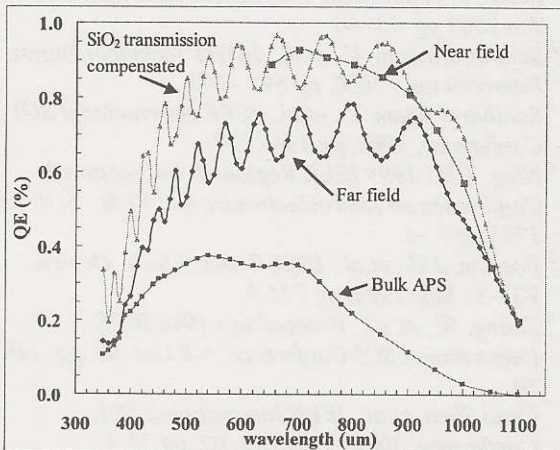

Figure 4: Measured QE of a photodiode fabricated in the SOI handle wafer indicates factor of 2-10x improved response compared to a bulk device over the wavelength range..

The spectral response is much flatter than that of a bulk-CMOS imager, because the low substrate doping yields a large depletion width (~16 µm) for field-aided carrier collection from deep in the handle wafer. The near-field data was taken using an integrating sphere. Thus, light input to the pixels was uniform in angular incidence, making the pixels more immune to fill factor loss. In contrast, the far-field measurements resulted in near-normal incidence that would be subject to fill factor issues. Indeed, the difference between the two sets of data corresponds well with the ~75% fill factor of the photodiodes. The interference pattern in the far field matches that expected from the passivation oxide.

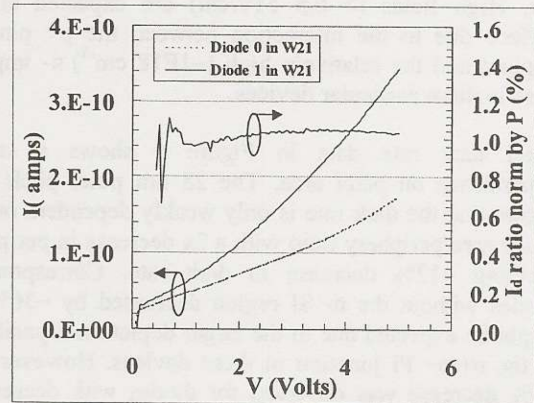

Figure 5: Flat voltage response of the ratio of dark current from two photodiodes, normalized by their perimeters(P), indicates a perimeter-dominated dark current. Diode leakage is ~10-20 nA/cm² area at 3 V, respectively.

Leakage current data obtained from two arrays of photodiodes, each totaling 1 mm², but with a 2x and 4x difference in perimeter and area, respectively, is shown in Figure 5. The results show a leakage current of ~1-20 nA/cm² over a 1-3V range. The presence of a field-dependent leakage current is indicative of a depletion-dominated process. The current dependence on voltage is seen to be perimeter, and not bulk, dependent. In wafers with higher pinning and surface implant dose, dark current depends super-linearly on the square root of the reverse bias voltage, pointing to possibilities of field-assisted tunneling or impact ionization near the

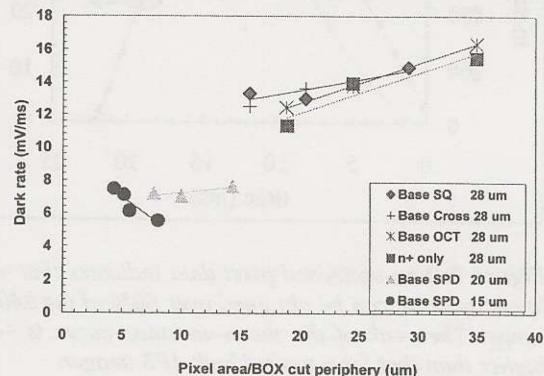

Figure 6: Dark rate data shows a strong dependence on pixel pitch (see legend). Pixel area is constant for each group, while the periphery changes by ~2x within a group.

surface. Data taken with guard a voltage >3V yield a flat dependence with voltage until breakdown at ~50V, also indicating the presence of localized high field regions within the photodiode that high guard voltages smooth out. High fields (> 0.5 MV/cm) are expected at the surface due to the interaction between the p+ pinning implant and the relatively high (~1E18 cm^{-3}) n- implant dose in these particular devices.

Pixel dark rate data in Figure 6 shows a strong dependence on *pixel* area. The 28 um pixel pitch data shows that the dark rate is only weakly dependent on the *diode* area/periphery ratio with a 2x decrease in periphery yielding ~12% decrease in dark rate. Corresponding diodes without the n- SI region decreased by ~36%, as might be expected due to the larger depletion capacitance at the n+/p+ PI junction in these devices. However, 45-65% decrease was observed for diodes with decreasing pixel pitch at a constant BOX cut size (i.e. constant diode area). The pixel area and diode periphery changes are both calculated with respect to the 28 um pixels for equivalent comparisons.

Data shown in Figure 7 indicates that pixel response is linear. Similar data has been observed for several of the test pixels. The mean-variance is also seen to be well-behaved with a peak variance ~4-5x higher than expected for bulk pixels, a result of the expected higher conversion

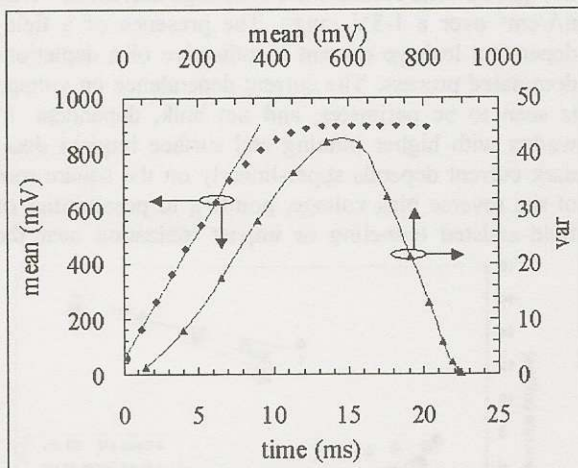

Figure 7: *Non-optimized pixel data indicates that ~4 % linearity error can be obtained over 80% of the 840 mV range. The peak of the mean-variance curve is ~4-5x higher than that for a typical bulk APS imager.*

gain of the SOI pixels. However, the conversion gain, estimated from the slope, is is more or less independent of diode area, and is primarily dominated by the edge capacitance formed between the highly doped pinning and surface implants, and a parallel source-to-body junction of the reset FET. This reveals a new trade-off in optimizing the pixel capacity.

Conclusion

In conclusion, we have demonstrated results for pixels made in the handle wafer of a SOI-CMOS technology. Measurements indicate fill-factor limited QE that is far superior to conventional pixels made using a bulk process. Similarly, red spectral response is particularly improved owing to the large collection volumes presented by the very large depletion regions. These front-illuminated results challenge back-illuminated CCD pixel response characteristics. Dark-current was higher than desired, and points towards the need for reoptimization of surface passivation implants to reduce surface electric field. The large depletion regions imply low cross-talk. Pixel linearity data are comparable with bulk CMOS imagers. These results suggest the possibility of implementation of high performance CMOS imagers SOI technology.

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