

Electroluminescence and Impact Ionization in CMOS Active Pixel Sensors

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ABSTRACT

In this paper, we analyze the effects of hot carriers (H-C) generation that occur in the in-pixel source follower transistor of CMOS APS pixels and show that it is associated with electroluminescence. These effects have been observed in several process generations ranging from 0.5 μm to 0.25 μm and various operating conditions.

It is shown that when a pixel is selected its follower transistor can generate excess minority carriers, and that a small amount of these charges flows towards the photosensitive area (or the diffusion storage node in snapshot imagers) to be collected. This implies a significant drop of the photodiode voltage when the amount of the collected carriers becomes larger than the junction leakage current.

1. INTRODUCTION

The requirements of both scaling down the pixel size of CMOS Image Sensor and maximizing its fill factor are commonly fulfilled by making use of deep submicron process and close-to-minimum size geometries for in-pixel transistors. However the impact of device scaling down in Active Pixel Sensors (APS) implies both advantages and drawbacks, especially the increase of parasitic currents¹. In CMOS imagers, additionally to the well-known thermal generation dark current, some degradations of the pixel response may be caused by other parasitic currents like hot carriers generation. Some of these currents come from the in-pixel source follower (SF) transistor operating in saturation i.e. the gate current, the gate tunneling current and the minority carriers generation by a secondary impact ionization phenomenon. By investigating the retention capability of a floating diode in a test pixel, an abnormal behavior was observed consisting of an excessive non linearity of the voltage response along time. Such a phenomenon was first observed in dynamic memory MOS IC's using junction capacitance as storage element, by Kudoh and al. in 1978². In this configuration, they noted an abnormal degradation of the holding time characteristics due to carrier generation of a transistor nearby the holding node

and explained it by the effect of the substrate current due to impact ionization at the drain of this transistor. From these results, we associated the excess non-linearity of CMOS-APS diode (being either the photodiode in 3T configuration or the floating junction retention node in 4T-shutter pixel) voltage variation with impact ionization currents. In 2001, Wang and al.³ has observed a similar phenomenon and explained it by the collection by sensitive area of excess minority carriers resulting from impact generation in the in-pixel follower transistor. In order to confirm the hot carriers production, we both analyzed the substrate current using models for H-C generation in MOS devices and looked for an associated electroluminescence. The latter was already observed on a readout circuit of an IR hybrid sensor⁴ and some of its consequences on devices and circuits were also demonstrated⁵. We investigated the effect of operating conditions on the H-C intensity and the closely associated electroluminescence and finally looked for its impact on neighboring pixels.

2. EXPERIMENTAL FACTS

Figure 1 shows a representation of photodiode pixels that have been investigated, including its readout circuit. The pixel unit cell consists of a photosensitive area (usually N/P junction) and three active transistors in the 3T configuration plus, in the 4T pixel, a shutter transistor that will allow the diffusion storage node to act as an analog memory.

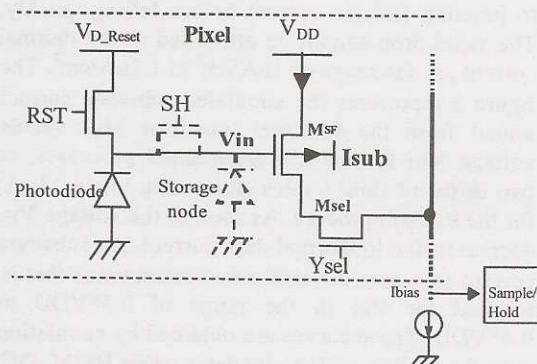


Figure 1: Schematic representation of photodiode pixel.

In order to visualize experimentally the hot carriers impact on the photodiode or storage node response, its voltage have been continuously monitored (through internal buffer), the pixel being selected by activating the transistor Msel. The figure 2 shows the photodiode voltage evolution in darkness along time, in the case of a Nwell photodiode pixel implemented respectively in standard 0.25 μm (area 62.2 μm^2) and 0.35 μm process (area 150 μm^2) at VDD=3.3V. Large integration time values are used to get significant variations of the photodiode at a room temperature.

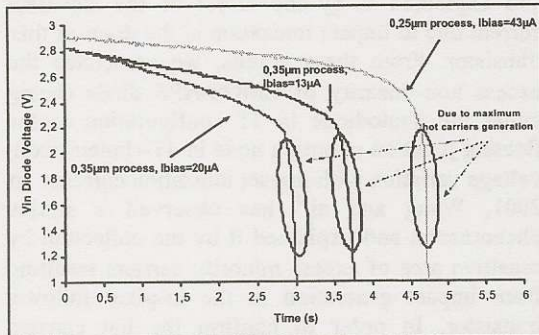


Figure 2: Photodiode voltage evolution in darkness along time in the case of a Nwell photodiode pixel implemented respectively in standard 0.25 μm (area 62.2 μm^2) and 0.35 μm process (area 150 μm^2) at VDD=3.3V.

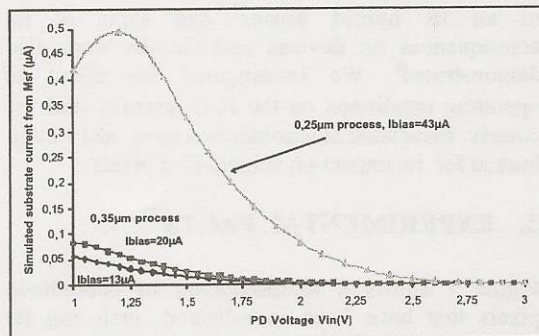


Figure 3: Simulated substrate current issued from the follower transistor Msf in standard 0.25 μm (Msf: W/L=1.6/0.35) and 0.35 μm process (Msf: W/L=1.1/0.45) at VDD=3.3V.

In these operating conditions, only parasitic currents discharge the photodiode. Figure 2 shows that, at first, the voltage Vin decreases slowly due to junction leakage current before falling quickly. The rapid drop cannot be attributed to the thermal current, in the range of 1nA/cm² to 1.2nA/cm². The figure 3 represents the simulated substrate current issued from the follower transistor Msf versus voltage Vin for the aforementioned processes, at two different Ibias values (Ibias=20 μA and 13 μA) for the 0.35 μm process. As soon as the voltage Vin decreases due to thermal dark current, the substrate current increases towards a maximum value that is reached for Vin in the range of 0.3*VDD to 0.4*VDD. These curves are obtained by simulation with the ELDO analog simulator using BSIM 3V3 MOS model that gives the precise description of the

substrate current, the substrate current Isub of one transistor being experimentally individually non measurable. The increase of the bias current value Ibias induces a higher substrate current and a higher minority carrier generation that makes the voltage Vin fall faster. This bias current corresponds to the flow of electrons in the channel of the in-pixel source follower transistor and the substrate current is directly dependent on it. As we will see in the next sections, this implies the generation of minority carriers that can flow through the substrate and can be collected by the photosensitive area.

3. HOT CARRIERS GENERATION

3.1 General aspects of hot carriers generation in a nMOS transistor

Impact ionization is a collision phenomenon where electrons gain enough energy (hot carrier) from an electric field to ionize silicon atoms and create electron-hole pairs.

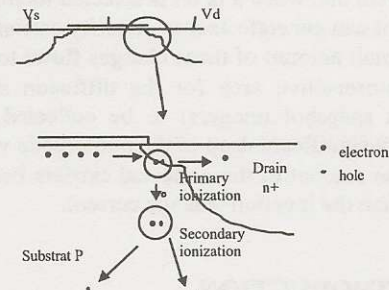


Figure 4: Primary and secondary impact ionization in a nMOS transistor

In a nMOS transistor, the electric field increases from the source to drain. It is maximum near the channel-drain junction and its intensity depends on the voltages Vds, Vg, channel length L and drain engineering option chosen for the given technology. The channel electrons are accelerated by the electric field and so their kinetic energy rises. As it is shown in the figure 4, they can ionize the silicon atoms by collision (primary ionization) and involve an avalanche phenomenon when the created electrons and holes gain energy and generate new electron-hole pairs. Photoinduced generation⁶ and secondary impact ionization by hot holes induces holes that participate to the substrate current and electrons that become minority carriers in the substrate. The minority carrier current Id in the substrate is given by⁷:

$$I_d \dot{\propto} I_{ion}^{s*} I_{sub}$$

where Isub is the substrate current

I_{ion}^{s*} is the ionization integral $I_{ion}^{s*} = \int \dot{\alpha}_s^* dx$ where α_s^* is the effective ionization rate and x the horizontal axis.

3.2 Hot carriers generation in the in-pixel source follower transistor

In the readout circuit shown in the figure 1, the selection of the pixel is made by setting on the transistor M_{sel} . Thus a current flow in the in-pixel source follower transistor M_{SF} that allows to sample the value of V_{in} . In this case, the transistor M_{SF} operates in the saturation region. Physical 2D device simulations (ISE-TCAD environment) of the pixel behavior allow to locate clearly the hot carriers generation area at its drain (Figure 5). The condition of simulation are the following: the voltage V_{in} is put at a reference voltage by pulsing the gate RST and the transistor M_{SF} is biased by a current I_{bias} . The darker sections outside N+ diffusions represent the substrate current obtained by simulation. This result means that in the normal operation of the pixel, hot carriers generation can occur during the selection time at a level depending on the integrated charge.

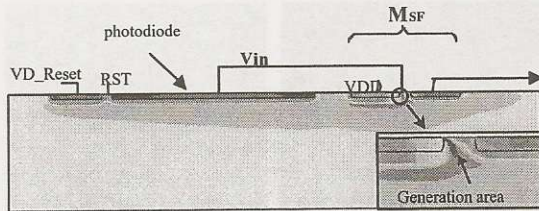


Figure 5: Physic representation of a part of a photodiode pixel with the ISE-TCAD software.

4. EFFECT OF HOT CARRIERS GENERATION ON PHOTODIODE CURRENT IN DARKNESS

The figure 6 gives the variation of the total current in darkness of a photodiode pixel (14 μm pitch) implemented using a 0.5 μm process (VDD=3.3V) versus the voltage V_{in} . It has been obtained from the photodiode voltage measurement. The pixel has a photosensitive area of 112 μm^2 .

This figure shows that the excess current in darkness has a strong variation with V_{in} and that it follows the hot carriers generation evolution given by the figure 7. This strong correlation indicates the collection of excess carriers by the photodiode: the hot carriers generation implies secondary minority carriers generation and the minority carriers (electrons) can flow through the substrate, reach a photosensitive area and thus affect its voltage response.

As hot carriers generation is related to electric field value at the drain, it strongly depends on the supply voltage power value VDD⁸. So it would be better to operate at the lowest supply voltage VDD, but this reduces the voltage swing of the sensor and its dynamic range.

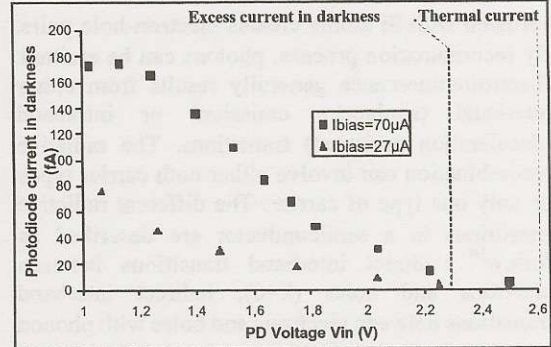


Figure 6: Photodiode current in darkness I_p versus voltage V_{in} at different currents I_{bias} (0.5 μm process, 14 μm pitch, VDD=3.3V, L=0.5 μm).

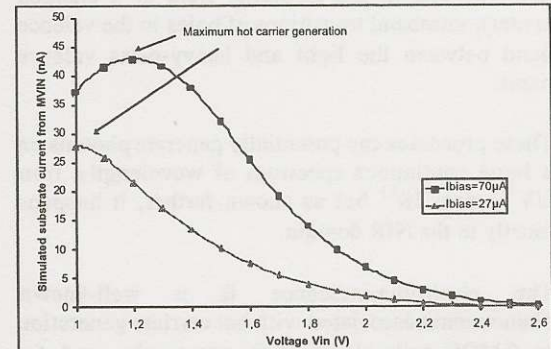


Figure 7: Simulated substrate current versus V_{in} voltage, issued from the follower transistor M_{SF} , curves obtained with ELDO analog simulation software at different currents I_{bias} (0.5 μm process, VDD=3.3V, L=0.5 μm).

5. ELECTROLUMINESCENCE AND HOT CARRIERS GENERATION

First observed by R. Newman in 1955⁹, the light emission from reverse-biased p-n junctions occurs when an electron at a higher energy state makes a transition to a lower energy state. When a radiative emission occurs, this results in a light emission called luminescence and the radiative efficiency is expressed as:

$$\zeta = \frac{R_r}{R_r + R_{nr}}$$

where R_{nr} is the non radiative recombination rate
 R_r is the radiative recombination rate

As an example, for a majority carrier density of 10^{17} at/cm³, the radiative efficiency η is $1.7 \cdot 10^{-5}$ for Si whereas it is 0.88 for GaAs, owing to the indirect gap of the silicon. So, the weak radiative transition probability in silicon makes this semiconductor not suitable as light source; nevertheless light emission from silicon is present and can be visualized.

Luminescence can occur when the system is not at the thermodynamic equilibrium. The electric field E of a transistor MOS does this job, the channel electrons are accelerated and their energy loss by

collision with Si atoms creates electron-hole pairs. By recombination process, photons can be emitted. Electroluminescence generally results from either interband (avalanche emission) or intraband (deceleration emission) transitions. The radiative recombination can involve either both carrier types or only one type of carrier. The different radiative transitions in a semiconductor are described as follow¹⁰ : direct interband transitions between electrons and holes ($k=0$); indirect interband transitions between electrons and holes with phonon emission ($k\neq 0$); intraband transitions of electrons in the conduction band (Photon-assisted electron transitions, Bremsstrahlung is breaking radiation of hot electrons in the Coulomb field at a charged center); intraband transitions of holes in the valence band between the light and heavy-mass valence band.

These processes can potentially generate photons on a large continuous spectrum of wavelengths from UV to near IR¹¹ but as shown farther, it happens mostly in the NIR domain.

The electroluminescence is a well-known phenomenon associated with hot carriers generation in CMOS technology; it is commonly used for failure analysis¹² such as localization of defect site (oxide rupture, ESD protection of a failed device). Many CMOS circuits are subject to luminescence without being disturbed but due to their nature, CMOS imagers can be sensitive to it. We have investigated the occurrence of electroluminescence in such devices. A dedicated setup has been developed; it consists of an optical microscope, a low light cooled CCD camera and a computer. This system has a spectral response from 330nm to 1100nm. The microscope and the device are placed in a black cage in order to avoid any external light to be detected by the CCD camera.

Electroluminescence has been initially observed in a 0.7 μm process but has also been found in a 0.5 μm , 0.35 μm and 0.25 μm processes. Figure 8 provides two examples of electroluminescence occurring during selection, when the input value corresponds to the maximum of hot electrons generation. It allows to see where the lighted area takes place, the white zone representing the emitting region that corresponds to the follower transistor region. Only a part of the generated photons can be measured, the remaining part going through the substrate and degrading the pixel response. The emitted light is so weak that transmissions loss from the emitting area to the low light cooled camera (passivation layer, objectives) degrade the visualization. So, long integration times with CCD camera are needed.

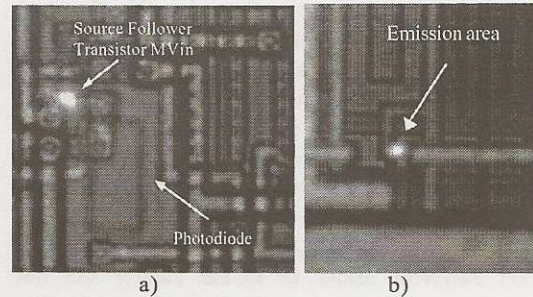


Figure 8: Light emission from a follower transistor of a selected pixel in a static operation.

a) 0.7 μm process VDD=5V ; W/L=2.2 μm /0.7 μm . Exposure time 60s. b) 0.25 μm process VDD=2.5V, Ibias=7.6 μA ; W/L=1.6 μm /0.35 μm . Exposure time 60s.

These figures demonstrate that photons can be generated by the source follower transistor during pixel selection.

As demonstrated by figure 9 obtained using passband filters, most of light emission occurs in the IR domain.

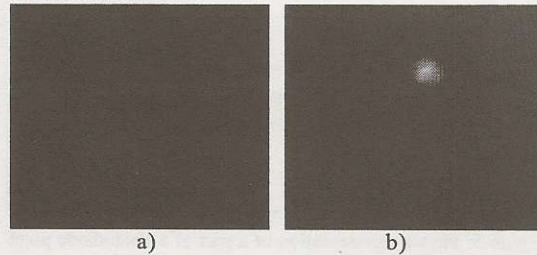


Figure 9: Light emission from a follower transistor in a 0.25 μm process with Exposure time 500s.

a) in the visible domain (up to 700nm) b) in the NIR domain (from 700nm)

Comparison of analog simulations of the substrate current from M_{SF} and measured photon emission demonstrates a strong correlation between the electroluminescence phenomenon and the hot carriers generation revealed by the substrate current (Figure 10 and Figure 11). The figure 10 gives the light emission using a 0.25 μm process with VDD=2.5V and Ibias=7.6 μA . The figure 11 is associated to a 0.5 μm process with VDD= 5V and two different Ibias values.

On the left vertical axis, the normalized light intensity from the follower transistor is represented and on the right vertical axis, the simulated substrate current from M_{SF} is given as a function of the voltage V_{in} . The light intensity of the luminescence depends on the gate voltage V_{in} of the transistor and we can notice that when the photodiode voltage V_{in} decrease, the light intensity from M_{SF} increases. So as for the minority carriers generation, the light emission increases non linearly with the decreasing voltage V_{in} . These figures prove that the light emission is associated with the hot electron effects in the source follower transistor of the readout circuit.

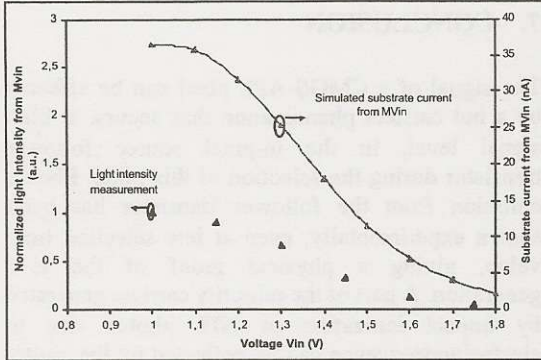


Figure 10: Correlation between the electroluminescence issued from the follower transistor M_{SF} and the simulated substrate current (0.25 μ m process VDD=2.5V, I_{bias} =7.6 μ A)

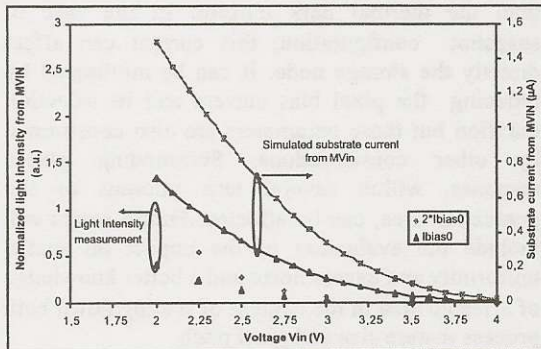
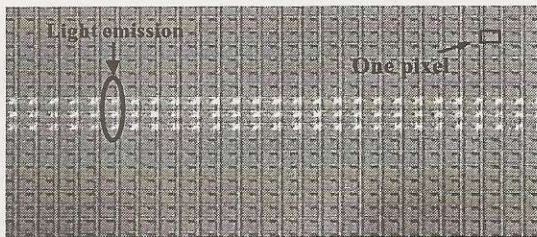
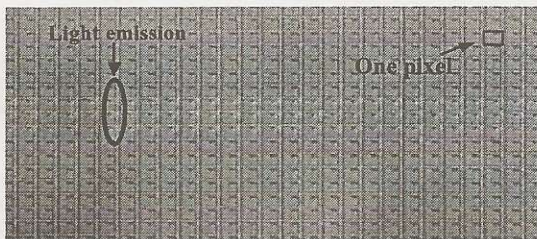


Figure 11: Correlation between the electroluminescence issued from the follower transistor M_{SF} and the substrate current at different I_{bias} (0.5 μ m process VDD=5V).

Figure 11 demonstrates the impact of bias current I_{bias} on photon emission. Increasing I_{bias} makes the hot carriers generation increase and so the generation of light too.



a)



b)

Figure 12: Electroluminescence from the source follower transistors when reading successively three different rows. (0.35 process, I_{bias} =13 μ A).

a) The selection duration is 203 μ s and the exposure time of the CCD camera is 150s ; b) The selection duration is 3 μ s and the exposure time of the CCD camera is 750s. Selection duration is 3 μ s.

One can legitimately wonder if H-C generation and electroluminescence occur for very short duration of current flow through M_{SF} (i.e. in practical operating conditions). The figure 12 shows the electroluminescence phenomenon from a pixel sub-array using a 0.35 μ m process (VDD =3.3 Volts, bias current 10 μ A). A word generator supplies the DUT with signals that allows three rows located in the middle of the sub-array to be continuously successively read out at 1Mpixel/s. N+/P photodiodes are used in classical 3T-pixel organization with a selection time of respectively 203 μ s and 3 μ s in the figures 12a. & 12b. The CCD camera exposure time is 150s (figure 12a.) and 750s (figure 12b.). We clearly see the light emission from the transistors areas located in the upper right corner of the pixel. Each selected pixel makes its source follower transistor emit light during the readout. The V_{in} photodiode voltage is set to a specified value (by the way of the isolated drain of the reset transistor), generating a significant hot-carriers amount.

So electroluminescence phenomenon occurs during a practical pixel readout and sampling phase, mostly at high signal level. In addition to a lower power consumption, minimizing the row selection time reduces the emission of parasitic light.

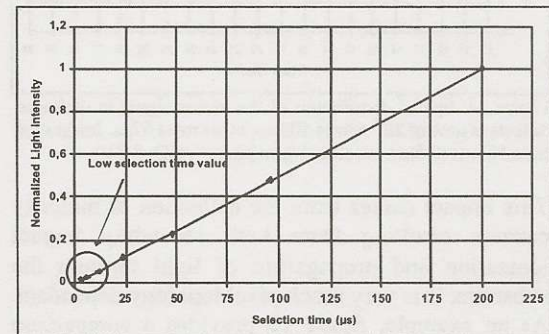


Figure 13. Normalized light intensity at different selection time value using a 0.35 μ m process with VDD=3.3V and I_{bias} =13 μ A.

The figure 13 represents the normalized light intensity from the in-pixel source follower transistor as a function of the row selection time. The sampling phase duration is the same at any point, only the selection time changes. One million row readouts has been performed during the CCD exposure time of 33 minutes.

It has to be noticed from figures 12b) and 13 that, even at short selection duration, electroluminescence occurs and can be visualized, demonstrating H-C generation in practical operating conditions.

Additional investigations will be focused on the impact of this H-C generation and electroluminescence phenomena in terms of disturbance in the surround of a selected pixel.

6. SPATIAL IMPACT OF EXCESS MINORITY CARRIERS

H-C generation and electroluminescence induce excess minority carriers that migrate through the substrate. By using a timing diagram that allows to select a row for a longer duration than the others, the spatial distribution of the excess minority carriers can be obtained. Thus, this line is very much affected by its own M_{SF} H-C generation when compared to all the others (being uniformly weakly disturbed by their own M_{SF}). All the array lines have the same integration time (508ms) but only the 20th line is selected for a longer duration (500ms), the other lines being selected 67 μ s. The figure 14 shows the spatial distribution of the measured excess signal for a 14 μ m pitch pixel in a 0.5 μ m process. The affected area by the excess minority carriers collection is within a range of 30 μ m of the generation area (in that case the 20th row).

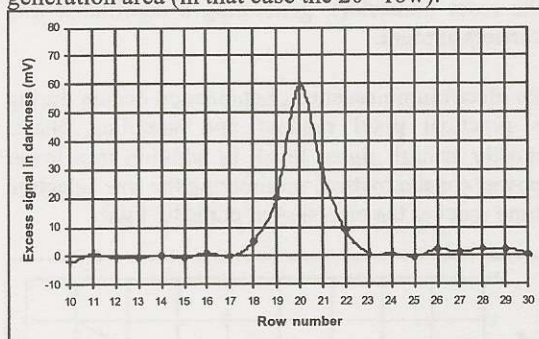


Figure 14: Spatial distribution of the excess signal in darkness. Selection time of 20th row is 500ms, other rows 67 μ s. Integration time 508ms (0.5 μ m process, 14 μ m pitch, VDD=3.3V).

This impact comes from the collection of minority carriers resulting from both secondary impact ionization and propagation of light through the substrate. It is very much pixel topology dependant. As an example, figure 15 provides a comparison between the photodiode and storage node voltage degradation in the case of a 4T_shutter-type pixel. One can notice that unexpectedly, while having a much smaller capacitance, the storage node voltage variation slope is lower than the photodiode one at high signal level.

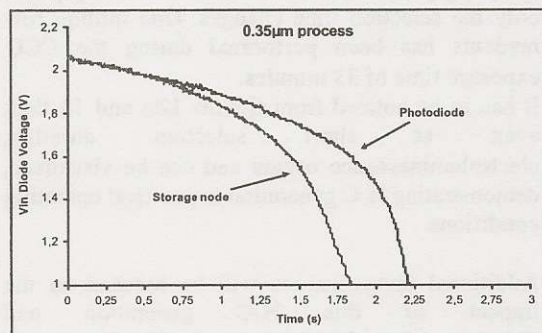


Figure 15: photodiode and storage node voltage evolution in darkness along time in the case of a 4T_shutter type pixel (0.35 μ m process VDD=3.3V).

7. CONCLUSION

The signal of a CMOS-APS pixel can be affected by a hot carriers phenomenon that occurs, at high signal level, in the in-pixel source follower transistor during the selection of this pixel. Photon emission from the follower transistor has been shown experimentally, even at low selection time value, giving a physical proof of the H-C generation. A part of the minority carriers generated by impact ionization or NIR photon due to electroluminescence can be collected by the photo-sensitive area or any diffusion storage node. These effects are measured as an excess current whose instantaneous value may be considerably higher than the thermal dark current. In the case of snapshot configuration, this current can affect directly the storage node. It can be minimized by reducing the pixel bias current and its selection duration but these parameters are also constrained by other considerations. Surrounding pixels response, within several tens microns of the generation area, can be affected. Future works will include the evaluation of the impact on spatial uniformity and excess noise and a better knowledge of affected area in the context of scaling down both process feature size and pixel pitch.

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