248-nm UV Damage Mechanism in MPP CCD's

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Abstract

CCD's can be damaged by exposure to 248-nm radiation. MPP (multi-pinned-phase) CCD's are more easily damaged than non-MPP CCD's. We will report on the mechanisms behind UV damage and explain why UV affects MPP CCD's more easily. We will present experimental results to corroborate our hypothesis.

I. Introduction

The scientific literature has a few reports on the stability of the CCD's to deep UV exposure [1], [2]. However, detailed analyses of the UV damage mechanisms are difficult to find.

Understanding the various UV damage mechanisms is important since this allows the design of sensors that are more tolerant of UV radiation. This also allows us to recommend modes of operation that makes the sensor least susceptible to UV damage.

The type and severity of UV-induced damage is a function of the wavelength of illumination, exposure conditions, the device structure, and the way that the device is operated during exposure. We will explore each of these separately.

II. Dependence on UV Wavelength

The higher the photon energy of the incident illumination, the more types of atomic level interactions are possible. Photon energy is a function of the wavelength of illumination. Table 1 lists some of the energy transition boundaries and absorption peaks that are associated with UV photons.

Some of the energy transitions are an inherent property of the material and are hence present all the time. Some are a result of non-idealities in the material structure and can therefore be minimized through proper processing.

One non-ideality that can be minimized through proper processing is color center formation. When UV photons break or rearrange bonds in SiO_2, the new bonds, radicals, and uncoordinated atoms formed have distinct photon absorption wavelength peaks. The new absorptive species are called color centers [3], [4]. Because UV photons modify the optical properties of materials, UV is commonly known to bleach materials.

E (eV)	λ (nm)	Comments
3.2	387	Si $E_C \rightarrow SiO_2$ E_C
4.3	288	Si $E_V \rightarrow SiO_2$ E_C
4.7	264	Si $E_V \rightarrow SiO_2$ E_V
4.7	264	Absorption peak of $P(O\text{-}Si)_5$ color center in $P_2O_5\text{-}SiO_2$ glass
4.8	260	Absorption peak of non-bridging O hole center in SiO_2
~5.0	~248	Si_3N_4 bandgap
5.1	243	O_2 dissociation begins
5.8	215	Absorption peak of uncoordinated Si in SiO_2
7.6	163	Absorption peak of peroxy radical in SiO_2
9.0	138	SiO_2 bandgap

E_C = Conduction Band, E_V = Valence Band

Table 1. Silicon-oxide energy transitions and absorption peaks in the UV.

The rate color center formation in SiO_2 is a function of the OH content of the oxide, along with other variables that can be affected by processing. Here, we will assume that the oxide has been sufficiently optimized so that color center formation is either negligible or is occurring at a rate that is acceptable to the application.

As shown in table 1, UV photons can induce many types of energy transitions. We will limit

this scope of this manuscript to changes that can be induced by exposure to 248 nm photons.

II. Exposure Conditions

The rate of UV-induced change to material properties is normally not a linear function of UV fluence. The fact that there can be many concurrent processes, each with its own dependence on UV fluence, complicates the interpretation of many experimental results.

To limit the scope of this manuscript, we will only report on the damage characteristics observed after devices are exposed to approximately 3 J/cm^2 of 248-nm radiation.

III. Pixel Structure

The devices exposed to UV are 13-μm-square-pixel frontside-illuminated poly-gate CCD's as shown in Figure 1. Openings in the polysilicon allow 248-nm photons to be collected by the buried channel potential well of the CCD.

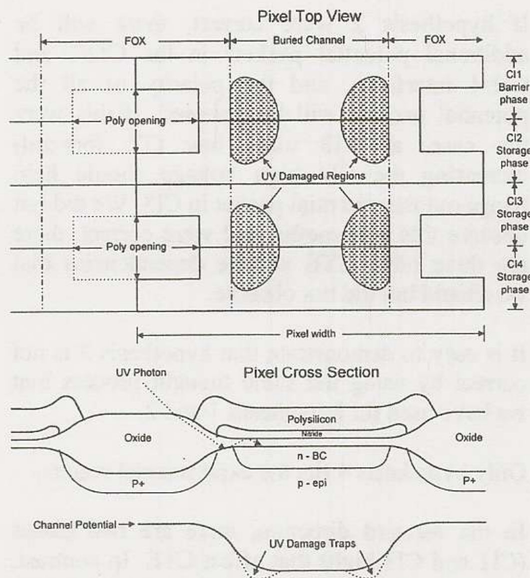

Figure 1.
UV Damage Location in the Photosite.
The figure is drawn for illustrative purposes only. Dimensions are not drawn to scale.

The barrier phase – the phase with the lower pinned channel potential when all phases are pinned – is CI1. It is important to remember this when we discuss the results below.

IV. Damage Observed

We observe degradation in CTE after prolonged exposure to UV.

Charges in this CCD can move in either the forward or reverse direction. We use the following as a convention. Using Figure 1 as a reference, in the forward direction, charges move from the top to the bottom of the array. In the reverse direction, charges move from the bottom to the top of the array.

The poorer the CTE, the greater is the amount of deferred charge on the first overclock line. Because each pixel column will have different level of CTE degradation, the first overclock line of a damaged sensor will have a unique deferred charge signature. We observe that this deferred charge signature is different in the forward and reverse directions.

We can improve the CTE of a damaged sensor by adjusting certain clock voltages. Table 2 lists the clock voltages that affect CTE. Note that the low voltage is unlikely to affect the CTE since the CCD is pinned when the clocks are biased low in the MPP mode.

Transfer Direct'n	Clock Voltage	Voltage Increase or Decrease	Effect on CTE
Forward	CI1 High	Increase	Improves
Forward	CI3 High	Increase	Improves
Reverse	CI2 High	Increase	Improves
All other combinations			No effect

Table 2. MPP clock voltages that affect the CTE of UV-Damaged Devices.

There is no sign of CTE degradation when a UV-damaged device is operated in the non-MPP mode.

If the same device is operated in the non-MPP mode during UV exposure but operated in the MPP mode during CTE measurement:

1. There is no sign of CTE degradation if the surface is depleted of carriers during UV exposure.
2. There is CTE degradation, albeit of a different signature, if the surface is filled with electrons during UV exposure.

Exposed surface-channel FETs in the CCD

amplifier exhibit a positive threshold voltage shift following prolonged UV exposure. Buried-channel FETs operating at least partially in the accumulation mode also exhibit a positive threshold voltage shift.

V. Hypotheses

We came up with four damage mechanism possibilities.

Hypothesis no. 1: UV photons transmit through the polysilicon gates and reach the $Si\text{-}SiO_2$ interface, where they can generate negative oxide traps. Adjacent poly gates overlap at gate boundaries, creating a thicker poly stack at that transmits less UV at gate boundaries. The non-uniform shift in threshold voltage results in potential packets in the CCD [5].

Hypothesis no. 2: The same as hypothesis no. 1, with the exception that the oxide traps generated are positive.

Hypothesis no. 3: The polysilicon gates absorb all 248-nm photons. However, some 248-nm photons still reach the $Si\text{-}SiO_2$ interface underneath the poly gate through internal reflection, as illustrated in Figure 1. Once the 248-nm photon is absorbed in silicon, it has sufficient energy to excite electrons into the oxide.

Hypothesis no. 4: The same as hypothesis no. 3, except that holes are excited into the oxide.

VI. Explanation of Experimental Results

Figures 2 and 3 illustrate the potential well diagrams in the forward and reverse modes respectively. The poly openings straddle CI1 and CI2, as well as CI3 and CI4, as shown in Figure 1. We marked the locations of the poly openings using dark boxes above the poly gates. The dark boxes in the potential wells indicate the locations of the potential traps. Although we have drawn the trap location and polarity to be consistent with hypothesis no. 4, it is fairly easy to mentally modify the picture to fit the other three hypotheses.

If hypothesis 1 were correct, the potential well is similar to that shown in Figures 2 and 3, but with additional potential packets between CI2 and CI3, as well as between CI1 and CI4. In the forward direction, as CI3 turns low, charges will be trapped in the CI2/3 interface. It will be advantageous to increase the CI4 high voltage to fringe out this trap. We did not observe any CTE improvement when we increased CI4 high however. Similarly, increasing the CI2 high voltage will help fringe out any trap in the CI1/4 interface in the forward direction. In the reverse direction, increasing the CI3 high voltage will help fringe out any trap in the CI1/4 interface and increasing the CI1 high voltage will help fringe out any trap in the CI2/3 interface. We did not observe these also.

Furthermore, if hypothesis 1 were correct, since the source of most of the negative traps has to be the photogenerated electrons, we should observe the same damage even if the sensor is operated in the non-MPP mode during UV exposure. Non-saturated sensors operated in the non-MPP mode during UV exposure do not exhibit CTE degradation even when subsequently operated in the MPP mode. This suggests that charge trapping does not occur when the surface is depleted of carriers.

If hypothesis 2 were correct, there will be additional potential packets in the CI2/3 and CI1/4 interfaces, and the polarity of all the potential packets will be reversed. If this were the case, as CI3 turns low (T2 forward) increasing the CI4 high voltage should help fringe out the potential packet in CI3. We did not observe this. If hypothesis 2 were correct, there are three other CTE voltage dependencies that we should but did not observe.

It is easy to demonstrate that hypothesis 3 is not correct by using the same thought process that we have used for hypotheses 1 and 2.

Only hypothesis 4 fits the experimental results.

In the forward direction, there are two biases (CI1 and CI3 high) that affect CTE. In contrast, there is only one bias (CI2 high) that affects CTE in the reverse direction. This asymmetry is a result of the asymmetry in the location of the poly openings. On the T3 forward direction, the difference in the CI1 and CI2 high potentials can cause charges trapped in the CI3/4 interface to fringe the wrong way, i.e. back to CI2. The same does not happen in the reverse direction because there is no poly opening in the CI2/3 interface. If hypotheses 1 or 2 were correct, there should be no asymmetry in the number of biases that affect CTE in the forward and reverse directions.

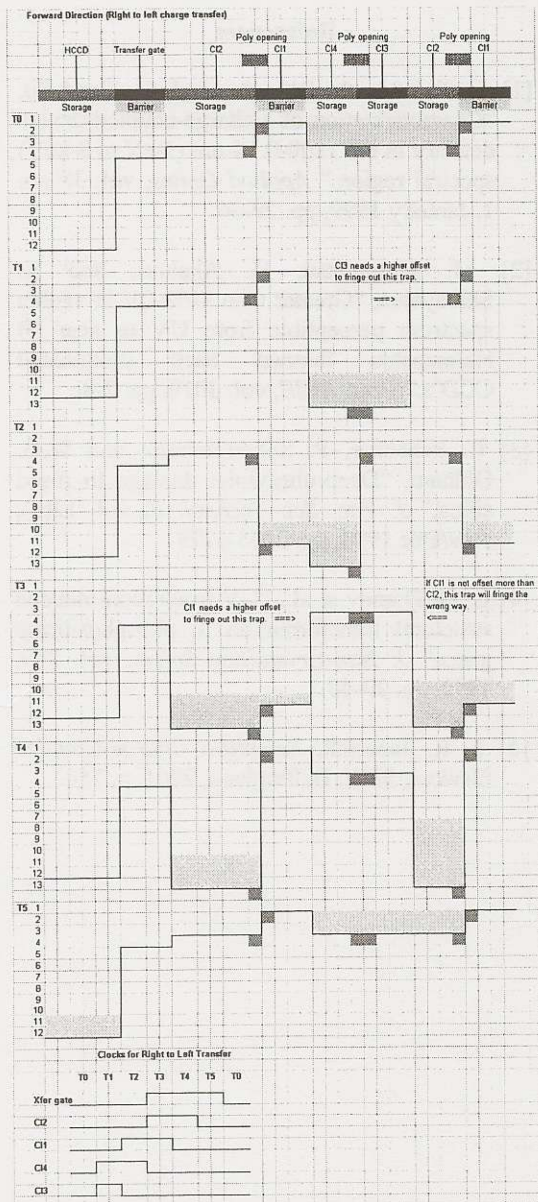

Figure 2.
MPP CCD potential well diagram illustrating UV-induced potential packet locations. Forward direction charge transfer is shown. The dark boxes in the potential well indicate potential trap locations.

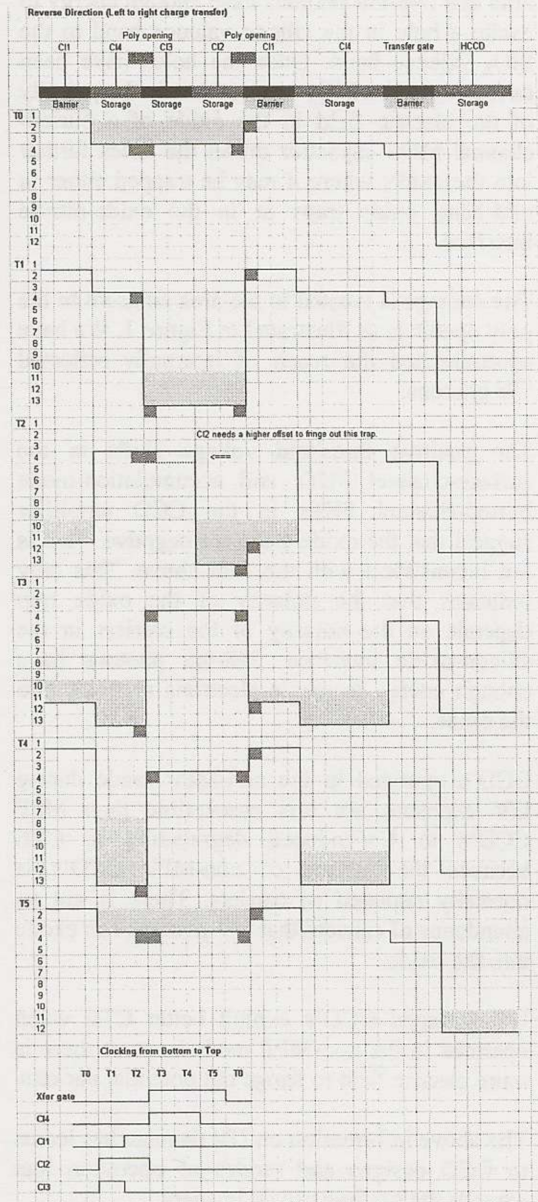

Figure 3
MPP CCD potential well diagram illustrating UV-induced potential packet locations. Reverse direction charge transfer is shown. The dark boxes in the potential well indicate potential trap locations.

Positive charge trapping is consistent with the fact that during integration, the surface of the MPP CCD is filled with holes. From Table 1, we note that 248-nm photons have enough energy to excite a hole in the silicon valence band to the SiO_2 valence band. Once the holes have been excited into the SiO_2 valence band, the polarity of the electric field in the oxide of a buried-channel MOS capacitor draws the holes further into the oxide, where it may be trapped either in mid-band oxide traps or in the oxide-nitride interface.

The damage is located in the area adjacent to the poly openings as illustrated in Figure 1. We have approximated the reach of internally reflected UV photons.

The positive threshold voltage shifts in the surface-channel FETs and accumulation-mode buried-channel FETs in the CCD amplifier suggest that the oxide traps are negative. This is not inconsistent with the data above. This only indicates that the polarity of the oxide trap depends on the polarity of the carriers in the silicon-oxide interface. 248-nm photons have enough energy to excite electrons or holes into the oxide.

CCD's operated in the non-MPP mode during UV exposure are less susceptible than MPP CCD's to UV-induced degradation in CTE because the surface of non-MPP CCD's is normally depleted of carriers. There is not an abundance of carriers that UV photons can excite into the oxide.

UV-damaged CCD's exhibit better CTE when operated in the non-MPP mode because there is more electric field to fringe out potential packets.

The above information on UV damage has led us to CCD designs and modes of operation that extends the lifetime of UV imagers.

VII. Conclusion

We have presented the mechanism by which MPP CCD's can be damaged by 248-nm photons. UV photons reach the Si-SiO_2 interface underneath CCD gates through internal reflection. When UV photons are absorbed, they can excite carriers into the gate oxide. The polarity of the oxide trap depends on the polarity of the carriers in the Si-SiO_2 interface. MPP CCD's are more susceptible to UV damage because the interface is filled with holes and because there is less electric field to fringe out UV-induced potential packets.

References

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