"R38" **1/2" 2Mpixel Full Frame CCD Sensor for Digital Photography**

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Abstract

A 2 million-pixel CCD sensor with 4.2μm x 4.2μm square pixels is designed using 0.4μm design rules, double polysilicon and double-metal technology. The sensor has a full-resolution imaging section with 5:4 aspect ratio and 8.6mm diagonal. In addition, a low-resolution storage section is included to operate the sensor as a frame-transfer device in the electronic viewfinder mode. Two different methods of vertical resolution reduction are implemented. The expected charge handling capacity obtained from the 3D analysis is 34000 electrons.

Introduction

Digital cameras require high-resolution image sensors to compete with traditional 35mm photography. Cameras with 2Mpixel sensors provide images that can be printed in full-page format with good resolution. In many applications digital cameras may be required to provide a lower resolution image in addition to their full resolution images. The operation of producing a sub-sampled image can be accomplished in the camera system itself at an expense of system complexity, additional cost and/or slow readout rates. However, if the reduction in resolution is accomplished in the sensor itself, the CCD can be operated at increased frame rates and the system becomes simpler.

Previously, a 2/3" 2-million pixel sensor with 5.6μm square pixels was designed and is in production. The architecture in this sensor provides both high-resolution still and low-resolution video images. Excellent pictures taken with this sensor demonstrate the performance of this technology, as well as proving the features of this architecture.

This current work focuses on the design of a 1/2" sensor of the same resolution and architecture for reduced cost and size. Since sensor performance has to be maintained while reducing the pixel size, extensive 3D analysis was done to optimize the scaled pixel design for maximum charge handling capacity and light sensitivity.

Imager Architecture and Fabrication Technology

Figure 1 shows the architecture of the image sensor that consists of the imaging section, storage section, horizontal register and output amplifier. The vertical clock voltage swing is 10V (+/-5V), horizontal clock voltage swing is 3.3V. The schematics of the three-stage source follower amplifier and details of the lower left corner of the sensor are shown in Figure 2.

The sensor can be operated in three different modes:

1) Mechanical shutter mode where exposure is controlled by opening and closing the shutter. Readout is done with no smear.
2) Hybrid shutter mode where exposure starts at the end of a frame injection cycle by turning the gates on and starting charge integration. The exposure ends when the mechanical shutter is closed and readout is done with no smear.
3) Viewfinder mode with electronic exposure control where smear is minimized by fast frame shift. The mechanical shutter is open for the entire period.

The sensor employs 4.2μm square pixels and is designed using double-polysilicon and double-metal technology with minimum features of 0.4μm. Two layers of polysilicon are used to create a 4-phase CCD. Polysilicon gates are strapped using titanium-lined tungsten metallization for reduced resistance. Metal straps run over the channel-stop regions, which consist of a p^+ doping and a thin field oxide. The pixel employs a profiled p-well implant to establish vertical overflow

drain. Chemical-mechanical polishing during metal-1 formation leaves an optically flat surface for color filters. The RGB, Bayer-mosaic patterned color filters are composed of dyed positive photoresist and are 1.2μm thick.

Design of Image and Storage Pixels

The pixels are designed in a 2 by 2 repeating pattern, matching the Bayer color filter pattern, as illustrated in Figure 3. The pixel fill-factor is 86%. The polysilicon gates are patterned to leave 22% open area for increased light sensitivity. The potential in these regions is controlled by a shallow p-type implant. A half-pixel wide and 2 pixel long structure used in the 3D analysis was created directly from the layout. The simulation result of a full potential well next to an empty potential well separated by a barrier gate is shown in Figure 4. The OFF gates are optimized so that the silicon surface is pinned by holes for reduced dark current and the potential barrier to the substrate is eliminated to enable the electronic reset operation. The p-well and buried channel implant doses are optimized so that the vertical antiblooming turns on before the device becomes surface channel or blooms to adjacent pixels. The potential barrier to the substrate ensures that there is no charge injection from substrate into the empty potential well under ON empty gates. Figure 5 shows one dimensional potential profiles as function of depth in the center of the pixel. The charge collection depth is 1.5μm. The charge handling capacity obtained from 3D device simulations with two gates ON is 34000 electrons. Transient analysis demonstrates perfect charge transfer and 100X blooming control.

The storage pixel is similar to the image pixel except that the polysilicon gates are not shaped to provide open areas. This results in a higher well capacity of 38000 electrons.

Selective Transfer of Image Rows to Storage Section to Implement Reduced Vertical Resolution

The architecture employed in this sensor provides two methods of reducing the vertical resolution during fast frame shift from the imaging section to the low-resolution storage section. The first method is to discard extra rows by injecting them into the substrate though the vertical overflow drain. The second method is to combine extra rows in the first row of the storage section.

The first method requires applying low voltage to S1 gates in the storage region while fast frame shift continues in the imaging region. Thus, any charge under the V4 gate of the last row in the imaging region is forced to inject to the substrate when this gate is turned OFF as shown in Figure 6. The CCD should be designed appropriately to ensure the whole charge is drained to the substrate with no blooming into the adjacent pixels.

Adding the signal of two desired rows reduces the vertical resolution while increasing the light sensitivity. To maintain color integrity, summing operation should comply with the repeating pattern of the color filter that has different color filters on successive rows. Rows of the same colors can be summed together but rows in between should be discarded. Summing takes place in the first storage row under S2 and S3 gates (Figure 7). While the image clocks shift normally, S1 turns ON and OFF allowing the new charge to combine with the previous charge in the first storage row. S2 and S3 gates are designed to limit the pixel charge to the maximum well capacity of the storage region. Any excess charge is drained to the substrate as S1 is turned OFF. It is important to make sure that the excess charge is drained to the substrate and does not bloom into the next pixel. This feature enables summation of as many pixels as desired.

Horizontal Register and Output Amplifier

The horizontal register is designed for progressive readout of the image through a single output. It has one four-phase stage per column of pixels. The register is designed for high charge transfer efficiency at frequencies up to 40 MHz with both 3.3 volt and 5 volt clocks. Simulations showed negligible charge transfer loss with clock swings as low as 2 volts. Calculated well capacity exceeds 50,000 electrons with 3.3 volt clocks.

The sense node and output structure are similar to those used on previous designs. Measured performance of this structure shows charge sensitivity of about 15 microvolts per electron at the output pin. The output buffer is a three-stage source follower design using surface channel devices for the amplifier transistors, and has a voltage gain of 0.6. Total equivalent noise from the output structure is less than 10 electrons in a 40 MHz bandwidth after correlated double sampling.

Summary

Scaling of CCD pixels in a given process technology affects the pixel in many ways. The reduced pixel size reduces the charge storage potential-well area and the stronger fringing fields reduce the potential-well depth. Optimization of the doping profiles used to create the potential-well can minimize the effect of fringing fields. The 3-D simulations we have performed have been able to eliminate this effect completely and increased the charge storage density from $1.6Ke^-/\mu m^2$ to $1.9Ke^-/\mu m^2$. Table-1 summarizes the measured parameters of the 2/3" and the design parameters of the 1/2" sensors. As shown on this table, the maximum well capacity of the pixel is not directly proportional to the area. Optimization of the doping profiles have also minimized the effects of scaling on the other structures in the sensor. The charge summing and clearing structure at the image-to-storage interface is still capable of clearing the undesired rows without causing blooming or leaving charge behind, and without causing CTE loss when rows of charge are transferred through it. The horizontal register with 3.3 volt swing maintained the required well capacity and CTE at high transfer rates.

In summary, a 1/2" 2Mpixel full frame CCD sensor for with 4.2 μm square pixels, capable of running in a reduced resolution mode, has been designed for digital camera applications. The sensor has good design performance matching requirements for the targeted applications.

	2/3"sensor (meas.)	1/2" sensor (design)
Chip Size (h x v) (mm)	7.4 x 7.5	9.9 x 10.0
Image pixel count	1609 x 1292	1609 x 1292
Total pixel count in image area	1680 x 1308	1680 x 1308
Storage pixel count	1680 x 262	1680 x 262
Image diagonal (mm)	11.6	8.7
Pixel size (μm)	5.6 x 5.6	4.2 x 4.2
Open area	21%	22%
Fill factor	75%	85%
Color filter pattern	Bayer	Bayer
Vertical shift freq. (MHz)	2	2
Horizontal shift freq. (MHz)	20	20
Max well capacity (e^-)	50K	34K
Conversion gain ($\mu v/e^-$)	15	15
Blooming suppression	>100X	>100X

Table 1. Comparison of 2/3" and 1/2" sensors

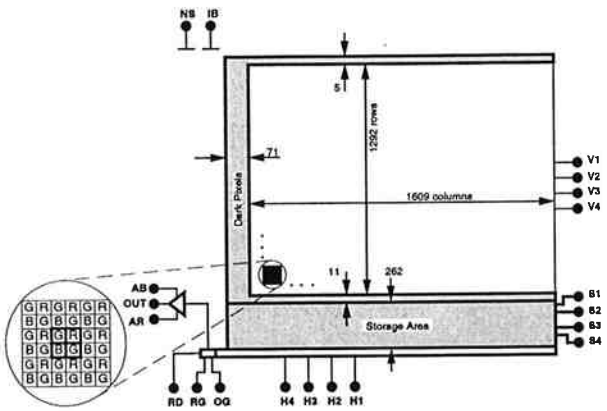

Figure 1. 2Mpixel sensor architecture.

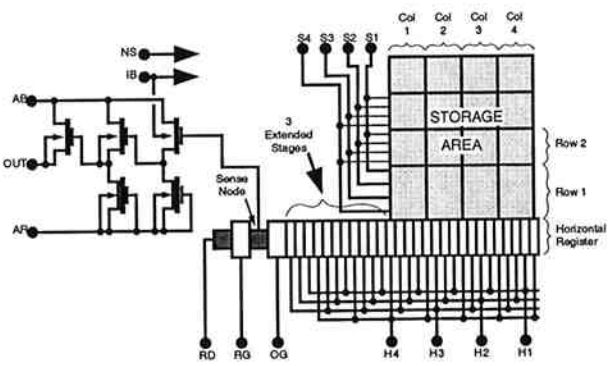

Figure 2. Schematics of the sense node and amplifier.

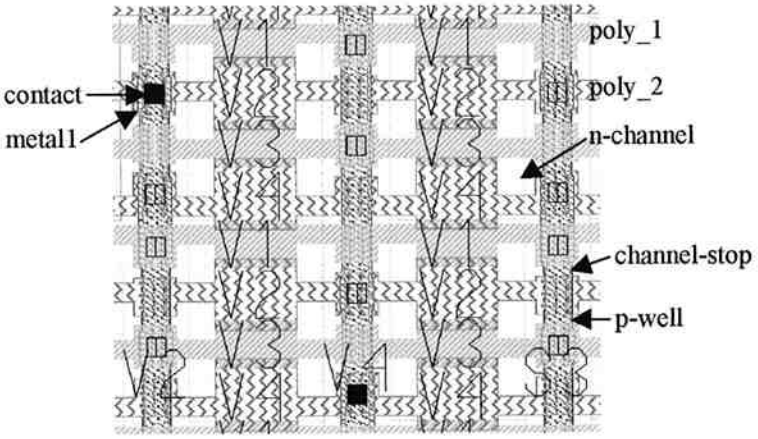

Figure 3. 2x2 pixel layout. Bayer color filter pattern is not shown.

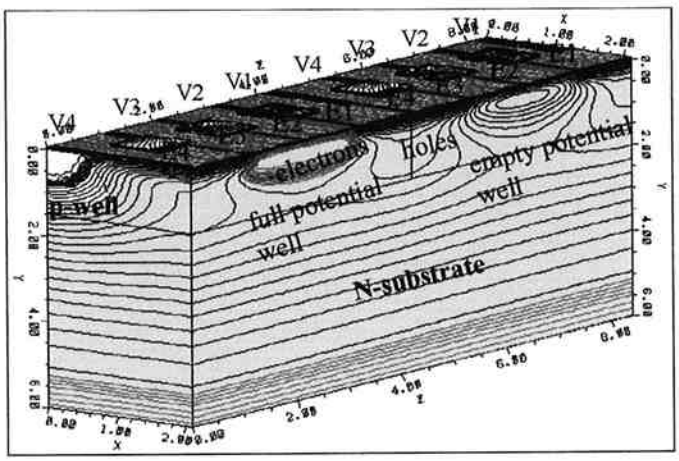

Figure 4. 3D simulation result of the half-pixel wide and two-pixel long structure.

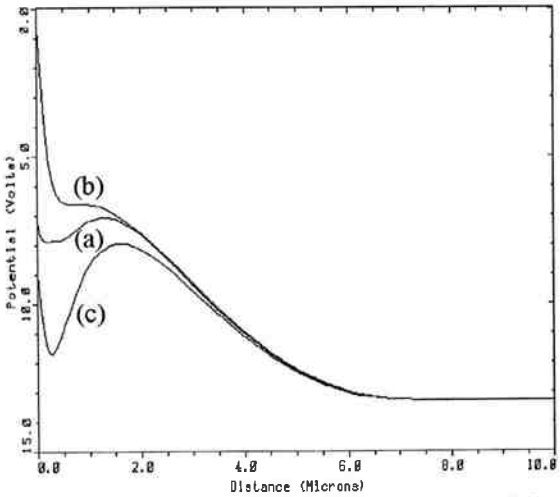

Figure 5. Potential profiles of (a) z = 2.1μm full potential well, (b) z = 4.2μm barrier voltage, and (c) z = 6.3μm empty potential well as function of depth.

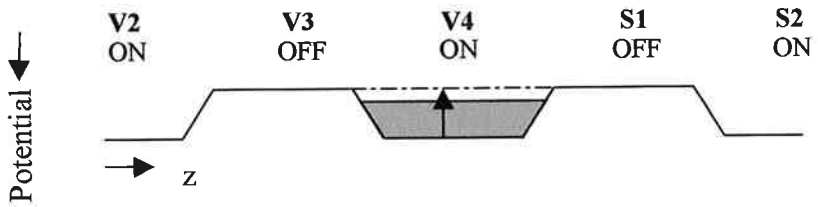

Figure 6. Line charge discarding by turning V4 gate OFF.

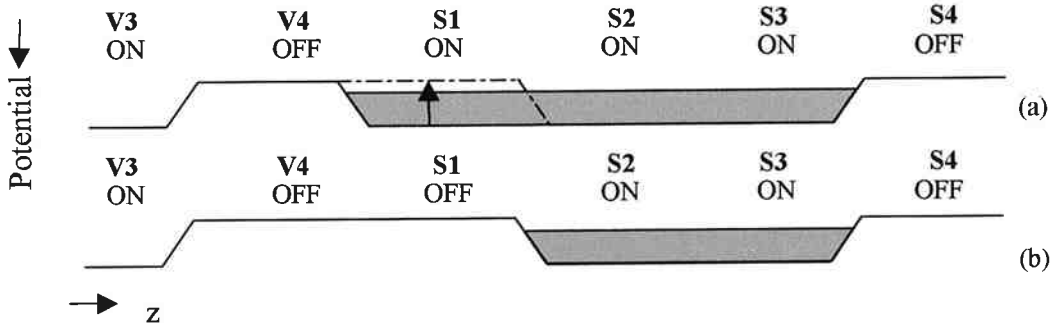

Figure 7. Summing the signal of two desired rows. (a) Signal of the two rows is transferred to the first storage row. (b) Excess charge is drained to the substrate by turning S1 OFF.