

CMOS Image Sensor overlaid with a HARP Photoconversion Layer

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1. Introduction

We have researched and developed a new CMOS image sensor with high sensitivity. The sensor has a stacked structure, i.e., HARP (High-gain Avalanche Rushing amorphous Photoconductor) film^[1] is overlaid on a CMOS readout circuit. This sensor is expected to have the following advantages compared with conventional CMOS image sensors and CCD image sensors.

- A larger signal can be obtained because of a large fill factor (almost 100%) and avalanche multiplication in a HARP film.
- Smear can be suppressed to a lower level because all incident light is absorbed in a HARP film.
- A large number of pixels can be integrated because photodiodes, which occupy a large area in each pixel, are not needed.

We have developed two technologies, i.e., those for a high-endurance voltage MOS transistor and an indium micro-bump process, to realize this sensor. A 128×128 sensor was fabricated and its characteristics were measured.

2. Configuration and Operation

A schematic diagram of the sensor and a cross-sectional view of a pixel are shown in Fig. 1 and Fig. 2, respectively. A HARP film is overlaid over the entire image area, and connects with a CMOS readout circuit through pixel electrodes. Holes generated by incident light in a HARP film are multiplied, then made to flow into a drain of an nMOS transistor (storage diodes) in each pixel. Signal holes are recombined with electrons in the drain, and the potential rises in accordance with light intensity. When a pixel is selected by scanners, the signal current of the pixel flows into a signal line. The signal is then amplified by line amplifiers arranged in each column, while noise is reduced by use of a CDS (Correlated Double Sampling) circuit to obtain a sensor output with a high signal-to-noise ratio.

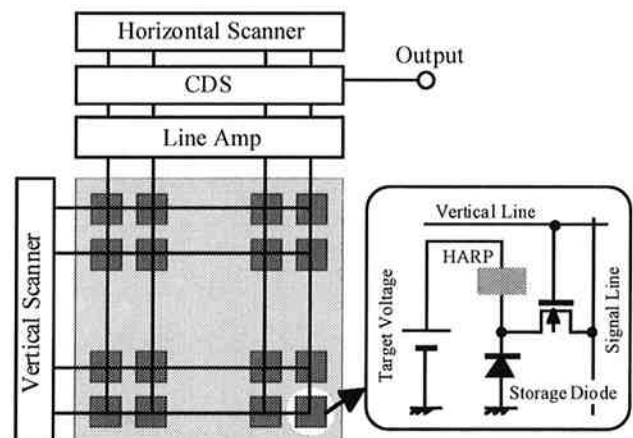


Fig. 1 Schematic diagram of the CMOS image sensor overlaid with a HARP photoconversion layer.

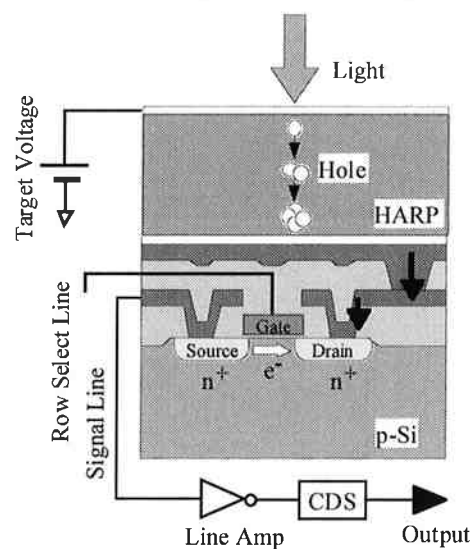


Fig. 2 Cross-sectional view of a pixel.

3. Key technologies

Technologies for the following were needed to realize this image sensor.

- Design and fabrication of a HARP film for a stacked solid state image sensor^[2].
- Increased endurance voltage of the MOS transistor.
- A new process to overlay a HARP film on a CMOS readout circuit.
- Noise reduction in the CMOS readout circuit.

The high-endurance voltage MOS transistor and new process to overlay a HARP film on a CMOS readout circuit had to be newly developed.

A high-endurance voltage MOS transistor^[3]

Drains of the MOS transistors arranged in each pixel connect with a HARP film through pixel electrodes. Therefore, when the sensor is exposed to strong light, the drain voltage might approach a target voltage that is applied to the HARP film, and so possibly cause damage to the drain of a conventional MOS transistor. We tried to increase the endurance voltage by using a new double-drain structure. A cross-sectional view of the high-endurance voltage MOS transistor is shown in Fig. 3. A low dose diffusion layer surrounds a conventional high dose diffusion layer. By using this structure, the impurity profile of the drain junction becomes gradual and the electric field around the drain is relaxed. A test transistor was fabricated and I-V characteristics were measured by setting a gate voltage of 0 V. The result is shown in Fig. 4. This shows that the endurance voltage of the MOS transistor has been increased to about 60 V, which is 3 times higher than that of a conventional one.

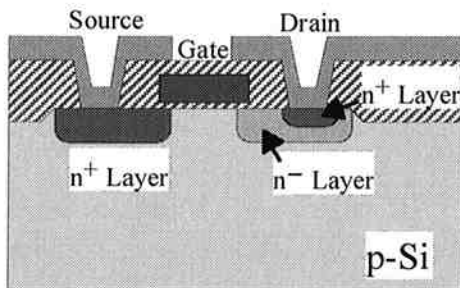


Fig. 3 Cross-sectional view of a high-endurance voltage MOS transistor.

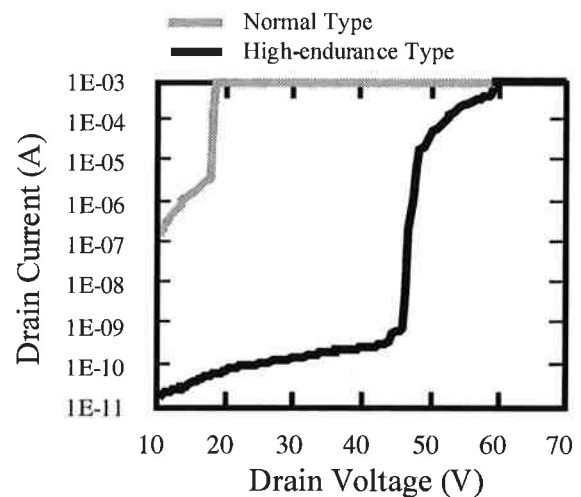


Fig. 4 Drain current versus drain voltage of a conventional and a high-endurance voltage MOS transistor.

Indium micro-bump process^[4]

Micro-bump electrodes have been adopted to provide contact with the HARP film on the CMOS readout circuit. The material of the micro-bump electrodes is indium. A cross-sectional view of the micro-bump contacts between HARP film and the CMOS readout circuit is shown in Fig. 5. It is important to form the indium micro-bumps uniformly on the electrodes in each pixel. To realize this, we have newly developed a lift-off process with two photoresist layers, and succeeded in

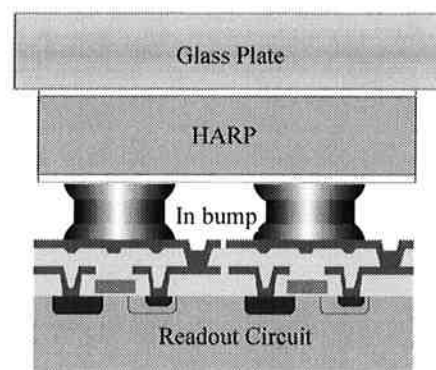


Fig. 5 Cross-sectional view of the indium micro-bumps between a HARP film and CMOS readout circuit.

forming uniform indium micro-bumps, $10\ \mu\text{m} \times 10\ \mu\text{m}$ in size and $5\ \mu\text{m}$ in height (Photo 1).

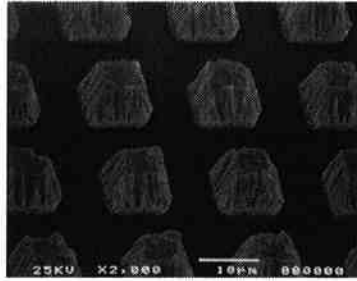


Photo 1 Indium micro-bumps fabricated by a lift-off process with two photoresist layers.

4. Design and Fabrication

The CMOS image sensor overlaid with a HARP film was designed and fabricated by using the new technologies described above and its basic characteristics were measured. The signal multiplication factor in the HARP film was designed to be 5 under a target voltage of 60 V, so thickness was set to $0.5\ \mu\text{m}$. The CMOS readout circuit was fabricated by use of a $2\ \mu\text{m}$ CMOS process. The size of the pixel is $15.4\ \mu\text{m} \times 15.4\ \mu\text{m}$, and the number of pixels is 128×128 . The image area is $1.97\ \text{mm} \times 1.97\ \text{mm}$.

5. Experimental Results

At first, in order to evaluate the characteristics of the HARP film itself, the relationship between the voltage applied to the HARP film and the current in the HARP film was measured by use of a 2/3-inch image pick-up tube. The result is shown in Fig. 6. This shows that a signal multiplication factor of about 5 has been achieved under a target voltage of 60 V as designed.

Next, we evaluated the characteristics of devices overlaid with a HARP film on a CMOS readout circuit. Fig. 7 shows the measured data which represent the relationship between the voltage applied to the HARP film and the output current under 3.1 lx and 5.0 lx illumination. Target voltage could be applied up to 65 V because of the low exposure level. This graph shows that avalanche multiplication starts under a target voltage of about 50 V and that the signal

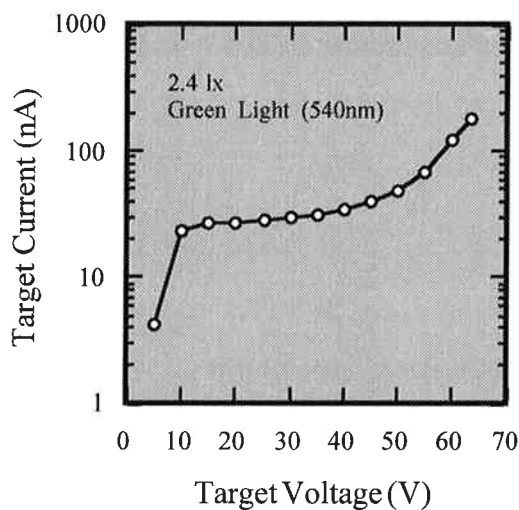


Fig. 6 Signal current versus applied voltage of a HARP film. It was measured under 2.4 lx illumination green light.

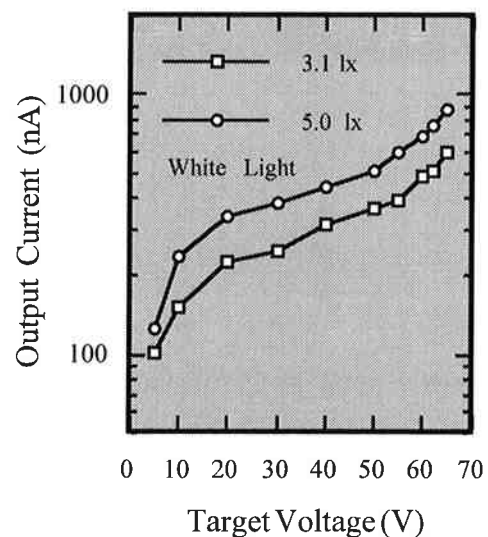


Fig. 7 Characteristics of the test device overlaid with a HARP film. These two curves were measured under 3.1 lx and 5.0 lx illumination white light.

multiplication factor is 2.5 under 65 V. This factor is about 0.4 times lower than the factor achieved in Fig. 6. We are investigating the cause of this phenomenon. The condition of the measurement, illumination and wavelength of light source, is different between Fig. 6 and Fig. 7, so we cannot compare them easily. Besides, it may be thought that effective voltage applied to the HARP film overlaid on the CMOS readout circuit reduces. Photo 2 shows a reproduced image which was taken under a target voltage of 60 V.



Photo 2 Reproduced image.

6. Conclusion

We have fabricated a 128×128 CMOS image sensor overlaid with a HARP film and confirmed signal multiplication in avalanche mode. The result demonstrates that this sensor may be expected to have high sensitivity. The characteristic of the HARP film itself was different from that when overlaid on a CMOS readout circuit. In the latter case, the multiplication factor was 0.4 times lower than in the original HARP film. It will be for future work to verify this phenomenon. It will also be important to decrease noise and achieve a higher signal-to-noise ratio.

References

- [1] K. Tanioka, J. Yamazaki, K. Shidara, K. Taketoshi, T. Kawamura, T. Hirai, Y. Takasaki, "Avalanche-mode Amorphous Selenium Photoconductive Target for Camera Tube," in *Advances in Electronics and Electron Physics*, 74, pp. 379-387, Academic Press (1988).
- [2] W. D. Park, Y. Takiguchi, M. Kosugi, M. Kubota, Y. Ohkawa, K. Miyakawa, S. Suzuki, K. Shidara, K. Tanioka, A. Kobayashi, T. Hirai, " An a-Se HARP Layer for a Solid-State Image Sensor," in *Proc. IEEE Workshop on CCD and Advanced Image Sensors*, Karuizawa, Japan, 1999.
- [3] M. Nakayama, H. Ohtake, M. Yamauchi, T. Tajima, M. Abe, " A High Voltage MOS Transistor for Solid-state Imager with Avalanche Multiplier Film," in *Proc. 1997 IEICE General Conference*, C-11-10, 1997; in Japanese.
- [4] T. Hayashida, T. Tajima, Y. Takiguchi, K. Kosugi, T. Watanabe, M. Abe, " Fabrication of Indium Micro-bump with Double Layer Photoresist Process," in *Extended Abstracts (45th JSAP Spring Meeting)*, 7-3, 1998; in Japanese.