R28 A Novel CMOS-APS Configuration With An Extremely Low Fixed Pattern Noise

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Abstract A novel CMOS-Active-Pixel-Sensor configuration, with an extremely low FPN, and with a high-speed readout time simultaneously, is proposed and evaluated successfully by the simulation. The proposed configuration has a Vth canceling ability in its pixel inherently, without any additional correction sequences, and with only one transistor increase in pixel components.

First, a new pixel configuration is proposed. It uses a Vth canceling technique similar to the current copier cell [1]. Second, a quantitative evaluation of the proposed pixel is made using an analog circuit simulation: (1) Reasonable operation of the proposed pixel is confirmed. (2) The first simulation gives a low FPN of 1/8 of the conventional-CMOS-APS value. And, (3) The reason for the residual FPN is solved. Then, the simulation obtains an extremely low FPN of 1/80 of the conventional-CMOS-APS value.

1. Introduction After solid-state sensors were introduced [2]etc, MOS image sensors were investigated and produced for camcorder use [3]etc. Meanwhile, amplification image sensors were proposed [4][5]etc. Recently, CMOS Active Pixel Sensors have newly been proposed, featuring new readout schemes that enables them practical and powerful means of image sensors [6]. However, the biggest drawback is ①the big FPN of several tens of mV. And, recently, effective readout schemes were proposed that reduce FPN to less than 1 mV [7][8]. Indeed these are excellent means of reducing FPN. However, ②the readout time increases considerably, which prevents higher-speed operation of CMOS APS's.

Until recently, circuits outside of the pixel did reduce FPN of CMOS-APS's. Let us make a new pixel with a FPN canceling ability in itself! In this paper, a novel extremely low-FPN pixel configuration is demonstrated.

2. Proposed-Pixel Configuration And Operation

Figure 2.1 shows a diagram of the conventional CMOS-APS pixel configuration. Photo sensing part is shown easily as a photodiode and a shutter transistor. As is widely known on the source follower circuit, output voltage Vout is Vout=Vpd-Vth. Where Vpd is the photodiode voltage and Vth is the MOS threshold voltage. This results in the big FPN, of the order of 30mVpp, due to the MOS Vth deviation.

The proposed pixel is shown in Figure 2.2. The pixel requires only one additional reset transistor, with its source connected to a reference voltage Vref. A reference current source Iref is also used. Both Vref and Iref are in outside of the pixel.

Operation of the proposed pixel cancels the MOS Vth voltage automatically from the output voltage, like the current copier cell [1]. Indeed this cell was utilized already in a readout circuit, as a high-resolution current mirror [9]. However, in this paper, the author points out another ability of this cell. That is "sampling and holding ability of Vth." This ability is "effectively involved and used inside the pixel".

Now, the operation sequence of the proposed pixel is shown. The sequence consists of basic steps only: (1)Reset, (2)Illumination, (3)Transfer and (4)Readout, without any additional correction steps.

(1) Reset: Φreset=high, Φshutter=high and Φrow=low

Figure 2.3 shows an equivalent circuit at the Reset timing. Transistors are shown as switches in order to understand easier. The reference current Iref flows through the amp tr. Ta to the reference voltage Vref. The gate-source voltage of Ta is fixed to the Vth that makes the drain current of Iref. The photodiode voltage Vpd at this timing, defined as Vreset, is given as shown below.

$$Vpd = Vreset = Vref + Vth \quad \cdots (1)$$

where Vth corresponds to the drain current of Iref. At this timing, the Vth is sampled and held in the photodiode.

(2) Illumination: Φreset=low, Φshutter=low and Φrow=low

Figure 2.4 represents the Illumination timing. Transistor switches are all in off state. After a determined illumination period, the photodiode voltage Vpd is given as follows.

$$Vpd = Vreset + \Delta V \quad (= Vref + Vth + \Delta V) \quad \cdots (2)$$

where ΔV is a photodiode voltage change due to the illumination.

(3) Transfer: Φreset=low, Φshutter=high and Φrow=low

Figure 2.5 represents the Transfer timing. The shutter transistor Tsh is turned on. Above Vpd is transferred and is held at the gate capacitance of Ta. The gate voltage Vg is given as follows.

$$Vg = Vpd \quad (= \text{above } Vpd) \quad \cdots (3)$$

(4) Readout: Φreset=low, Φshutter=low and Φrow=high

Figure 2.6 represents the Readout timing. The switching transistor Tsw is turned on. Vg is still held on above Vpd value. The amp transistor Ta functions as a source follower. The drain current of Iref flows to the output terminal Vout. Then, the output voltage Vout is given as shown below.

$$Vout = Vg - Vth \quad (= Vpd - Vth) \quad \cdots (4)$$

where this Vth also corresponds to the drain current of Iref. Then, the Vth is same to above Vth values. Consequently,

$$Vout = Vpd - Vth = Vref + Vth + \Delta V - Vth = Vref + \Delta V \quad \cdots (5)$$

As is shown above, the output voltage Vout of this pixel inherently does not contain MOS Vth value. Then, the MOS-Vth deviation problem does not affect the output-voltage deviation. Moreover, no correction sequences that reduce readout speed drastically are necessary.

Figure 2.7 shows the total circuit diagram of an area image sensor, using the proposed pixel.

3. Simulation The proposed pixel and the conventional pixel are evaluated using an analog circuit simulator PSpice®. Transistor models are of middle sizes in order to confirm the Vth-deviation effect on the output voltage clearly. (Wg=30 μm for NMOS and Wg=200 μm for PMOS. Lg=1 μm for both types.)

The photodiode is modeled as shown in Figure 3.1. The pulse current source supplies a current that corresponds to the photo current, for a period that corresponds to the illumination period.

Figure 3.2 shows the simulation circuit of the conventional pixel. External gate capacitance C1 of 5pF is used suit for medium transistor sizes. A current mirror is used as a load of the amp transistor Ta.

Expressions of pulse sources are like below: Pulse (initial voltage/current, pulse voltage/current, delay time, rise time, fall time, pulse width, period). Figure 3.3 shows the simulation circuit of the proposed pixel. Outer driver circuits are both current mirrors. In both figures, device parameters are chosen in order to make both operation conditions near equal.

Transient-analysis waveforms of the proposed pixel are shown in Figure3.4. On the horizontal axis, 0-0.5ms is the Reset timing. 0.5-0.9ms is Illumination, 1.0-1.2ms is Transfer and 1.5-1.7ms is Readout, respectively. A period of the 4-step cycle is 2ms. During the illumination, the Photodiode Voltage Vpd decreases around 2V. VOUT1, the Node voltage of node OUT1, is read as an output voltage, at 1.6ms on the horizontal axis.

Firstly, Output voltage deviations or FPN's are evaluated by Monte Carlo analysis. A device model parameter, e.g. Vth of Ta, is distributed in Gauss distribution. A histogram of VOUT1 is made.

Figure 3.5 shows the results for 30-times calculation, on the conventional pixel, due to about 30-mVpp in the Vth deviation of Ta. Central value of Vth is 1.5V. 1σ of Vth is 0.5%=7.5mV. (From $\pm 2\sigma$ to $\pm 2.5\sigma$, or 30-35 mVpp, is reasonable deviation width for 30-times calculation.) In the figure, VOUT1 deviation, or maximum − minimum, is 32.4mV that is nearly equal to the Vth deviation itself.

The proposed pixel produces a VOUT1 distribution, as is shown in Figure 3.6. VOUT1 deviation is 4.6mV that is nearly 1/8 of the conventional one. The Vth conditions, and the scale pitch of the horizontal axis in the figure, are as same as in Figure 3.5.

Secondly, results of the device-parametric analysis are summarized in Table 3.1. In each line of the table, or in each analysis, output-voltage deviation of the proposed pixel has reduced to 1/7-1/8 from conventional one.

4. Further FPN Reduction The reason for the residual output-voltage deviation is investigated and solved. Slight junction-capacitance difference of photodiodes between pixels, because of the slightly different reset voltages of photodiodes, due to the Vth distribution between pixels, is the main reason.

A constant-capacitance photodiode is promised to reduce the deviation further. Figure 4.1 shows the simulation model of the constant-capacitance photodiode. Output-voltage deviation of the proposed pixel, with the constant-capacitance photodiode model, is shown in Figure 4.2. VOUT1 deviation is 0.42mV that is 1/80 of the conventional pixel.

Figure 4.3 shows a practical constant-capacitance photo device, that is a reach-through diode structure, installed in the proposed pixel configuration.

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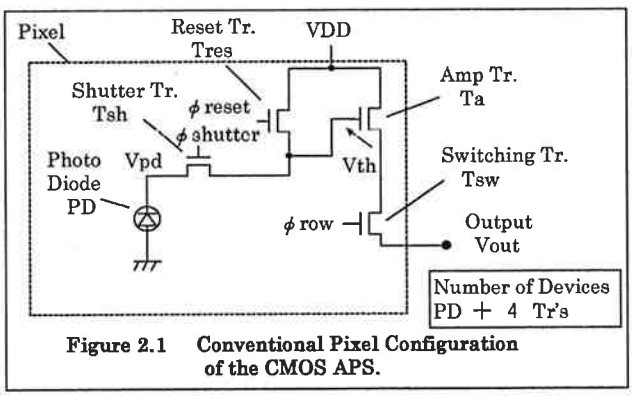


Figure 2.1 Conventional Pixel Configuration of the CMOS APS.

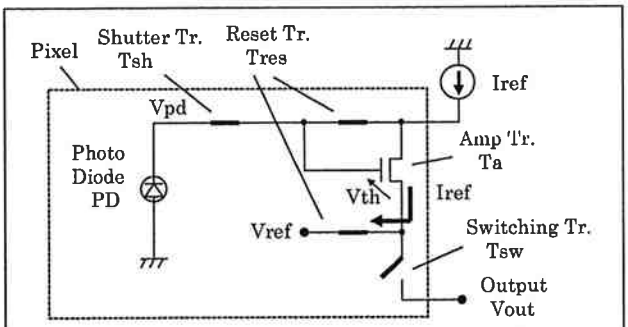


Figure 2.3 Equivalent Circuit at the Reset Timing.

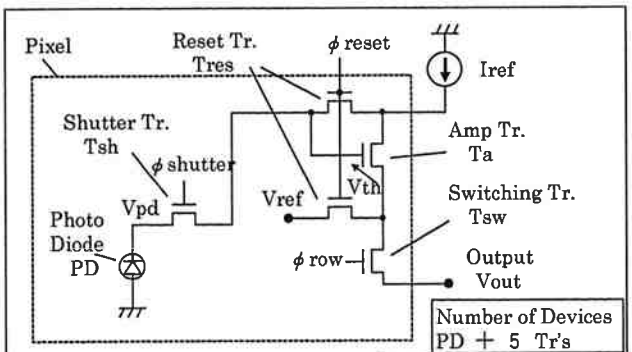


Figure 2.2 Proposed Pixel Configuration of the CMOS APS.

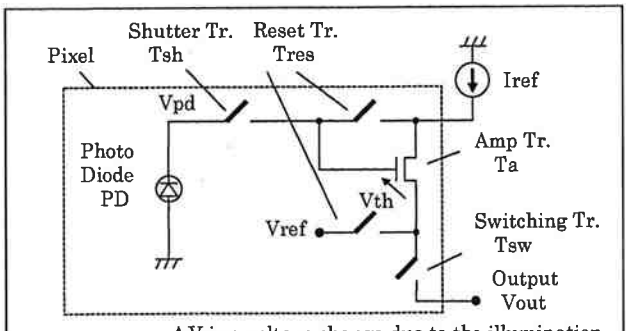
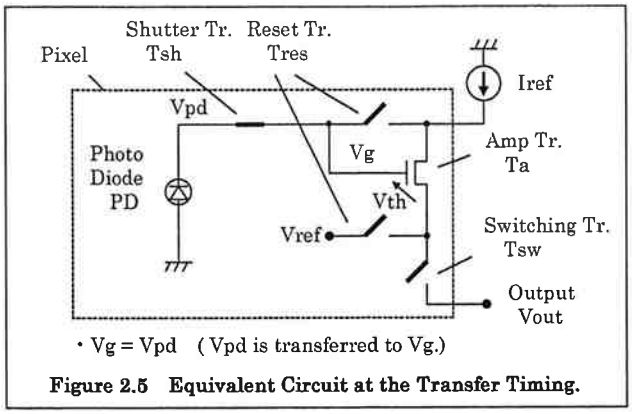
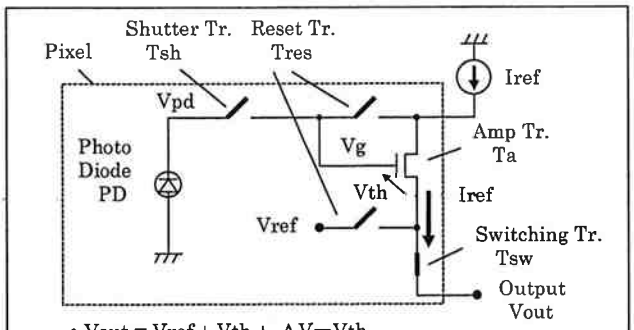


Figure 2.4 Equivalent Circuit at the Illumination.



• Vg = Vpd (Vpd is transferred to Vg.)

Figure 2.5 Equivalent Circuit at the Transfer Timing.



• Vout = Vref + Vth + ΔV−Vth
= Vref + ΔV (Vth is canceled.)

Figure 2.6 Equivalent Circuit at the Readout Timing.

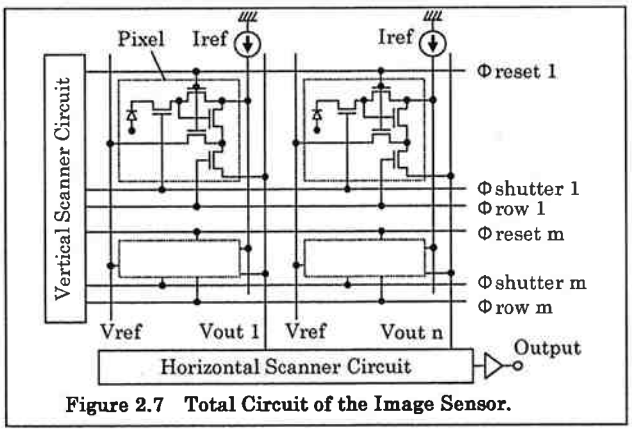


Figure 2.7 Total Circuit of the Image Sensor.

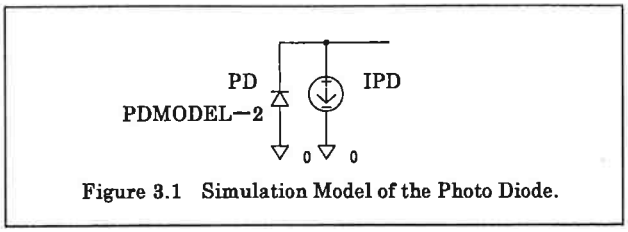


Figure 3.1 Simulation Model of the Photo Diode.

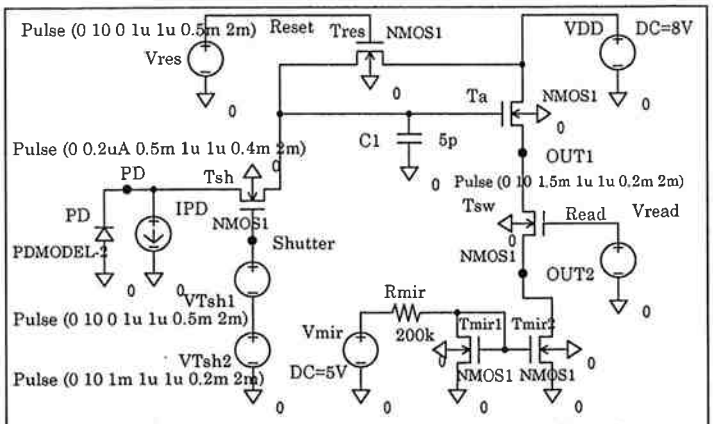


Figure 3.2 Simulation Circuit of the Conventional Pixel.

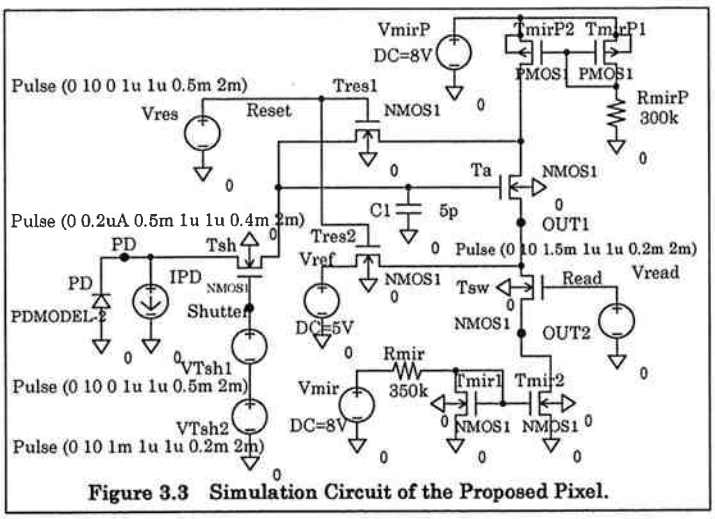


Figure 3.3 Simulation Circuit of the Proposed Pixel.

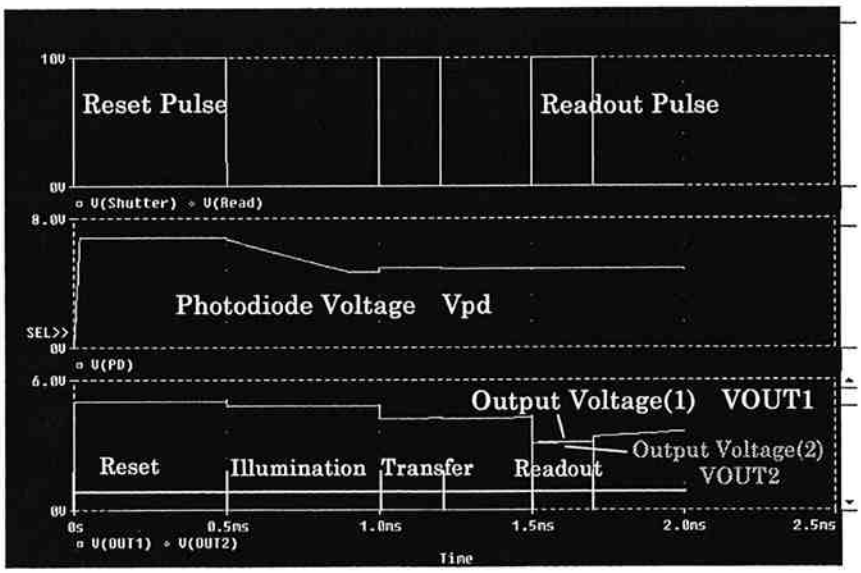


Figure 3.4 Transient-Analysis Waveforms of the Proposed Pixel.

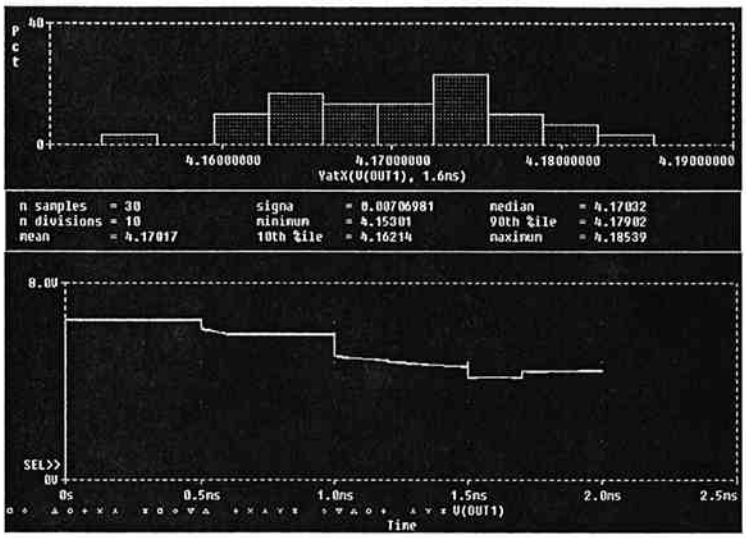


Figure 3.5 Output-Voltage Distribution of the Conventional Pixel due to the MOS Vth Deviation. (Monte Carlo Analysis.)

Table 3.1 Device-Parametric Analysis

Parameter	Central Value	Deviation	Deviation of the Output Voltage (= FPN)		Reduction of the Deviation (Prop./Conv.)
			Convention-al Pixel	Proposed Pixel	
Threshold Voltage Vth	(V) 1.5	(mV) ±15	(mV) 31.1	(mV) 3.9	1/8
Amp. Coefficient Kp	(μA/V^2) 20	(μA/V^2) ±2	(mV) 24.4	(mV) 3.1	1/8
Gate Length Lg	(μm) 1	(μm) ±0.1	(mV) 25.1	(mV) 3.7	1/7
Gate Width Wg	(μm) 30	(μm) ±3	(mV) 22.2	(mV) 2.7	1/8

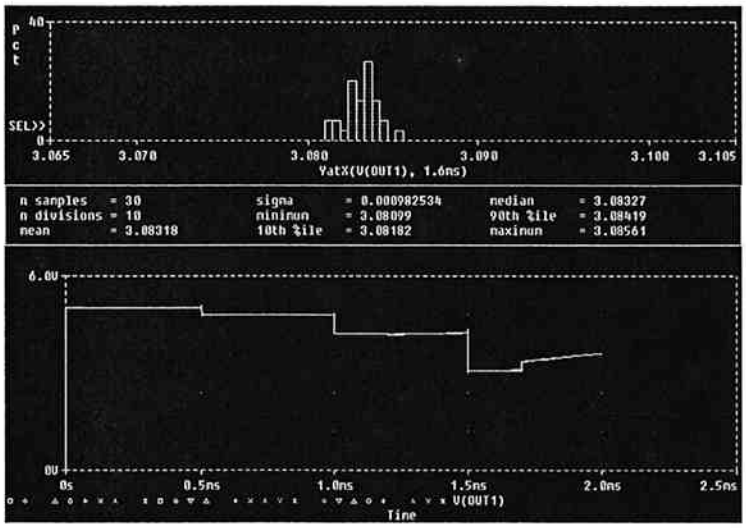


Figure 3.6 Output-Voltage Distribution of the Proposed Pixel due to the MOS Vth Deviation. (Monte Carlo Analysis.) (Same Scale Pitch to Figure 3.5.)

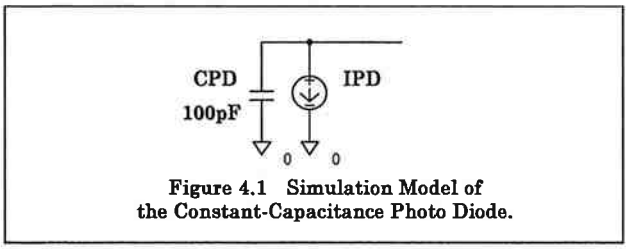


Figure 4.1 Simulation Model of the Constant-Capacitance Photo Diode.

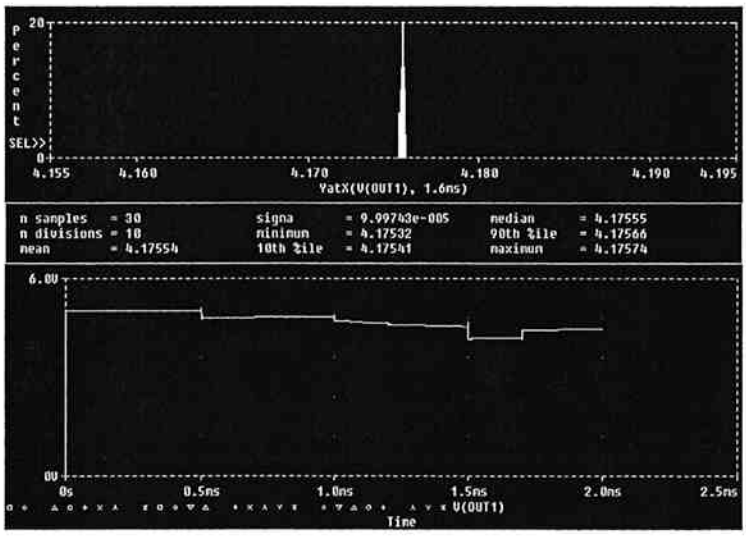


Figure 4.2 Output-Voltage Distribution of the Proposed Pixel, with the Constant-Capacitance Photodiode Model, due to the MOS Vth Deviation. (Monte Carlo Analysis.) (Same Scale Pitch to Figure 3.5.)

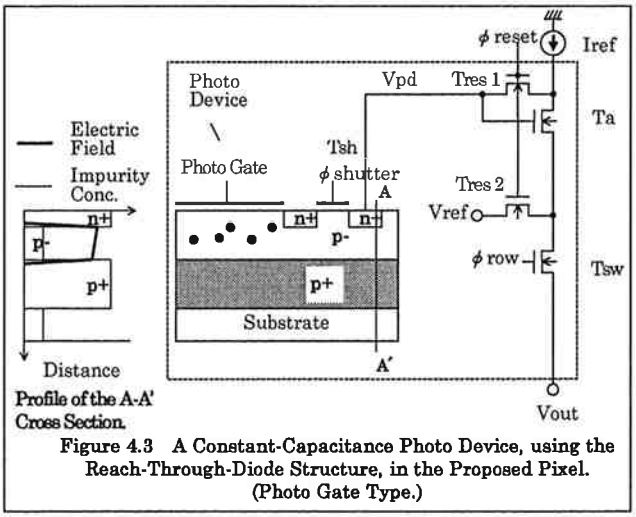


Figure 4.3 A Constant-Capacitance Photo Device, using the Reach-Through-Diode Structure, in the Proposed Pixel. (Photo Gate Type.)