R26: First Multispectral Diode Color Imager With Three Color Recognition And Color Memory In Each Pixel

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Abstract

A color image sensor without color filters has been successfully fabricated and tested for the first time. The novel TFA (Thin Film on ASIC) imager CAESAR (Color Array with Enhanced Sensitivity and Resolution) employs an amorphous silicon (a-Si:H) detector, the spectral sensitivity of which can be controlled through the applied bias voltage. The three linearly independent signals for red, green and blue sensitivity are stored inside the pixel and can be read out in parallel. First measurements revealed an excellent dynamic range and reasonable color separation.

Introduction

While the resolution of image sensors for digital photography will almost automatically increase with every new technology generation, the conventional approach to color recognition suffers from several drawbacks. CCDs are an efficient concept for high-resolution black & white imagers, however, additional efforts are necessary to allow color recognition. Multi-chip solutions with prisms or lens systems being too complex, consumer products mostly employ red, green and blue stripe or mosaic filters to recognize the primary colors on a single chip [1]. However, this technique requires a number of additional process steps, and the resolution is inherently limited. Moreover, back-side illuminated CCDs are necessary to achieve a high response also for short wavelengths.

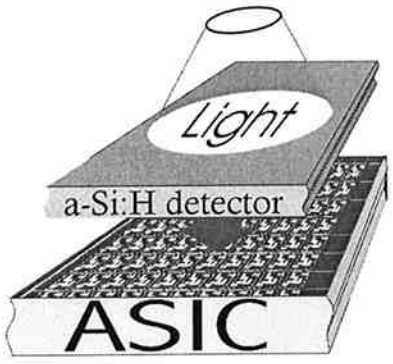

Fig. 1 TFA structure

TFA sensors employ an amorphous silicon thin film system on top of an ASIC. The two components can be optimized independently of each other, and a fill factor of up to 100 % is possible. The development of amorphous silicon detectors with adjustable spectral sensitivity renders color filters dispensable and leads to a cost reduction for color imaging. The spectral sensitivity of a CAESAR three color pixel is adjusted through successively applied bias voltages corresponding to blue, green and red detector sensitivity. In order to keep the exposure period duration short enough for single flash exposure, the blue, green and red signals are stored inside each pixel and read out simultaneously.

Photodetector

The a-Si:H thin film system of a TFA sensor is deposited onto the completed ASIC in a PECVD (Plasma Enhanced Chemical Vapor Deposition) process. While sequences with one intrinsic layer as the main collection region for absorbed charge carriers are employed for black & white sensors, further subdivisions are the key to color recognition [2]. In a suited layer system with a graded bandgap the main collection region proceeds to deeper intrinsic layers with increasing reverse bias between the top and bottom electrodes. In this way the detector is blue sensitive for small bias (0 V), green sensitive for moderate bias (-1.5 V) and red sensitive for higher values (-5 V).

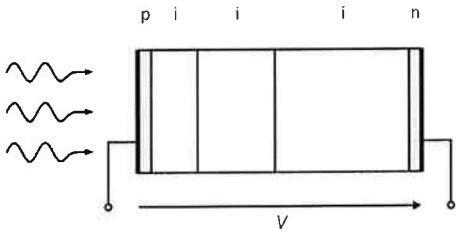

Fig. 2 a-Si:H color diode

Fig. 3 depicts the photo- and dark current characteristics of the CAESAR detector. The dynamic range, referred to 1000 lx illumination, is around 90 dB in the relevant voltage range from 0 to -5 V.

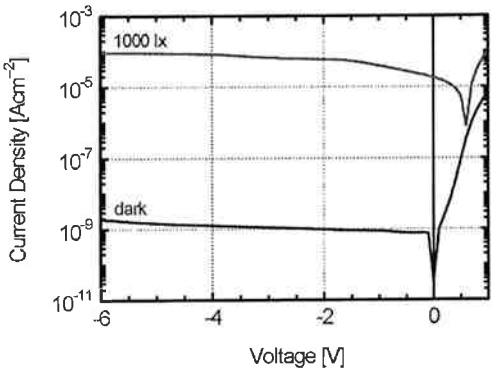

Fig. 3 I-V characteristics of CAESAR detector

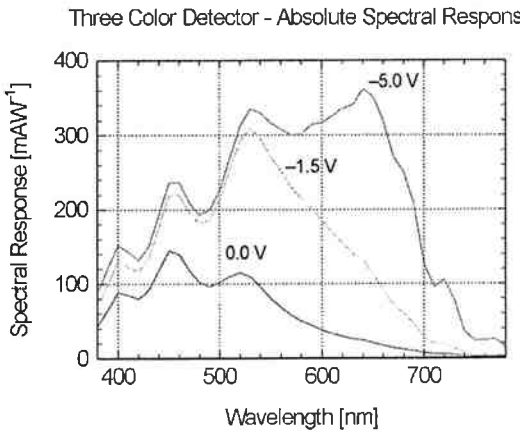

Fig. 4 Uncorrected spectral sensitivity of CAESAR detector

Fig. 4 demonstrates the voltage controlled variation of the spectral response. The peak responsivity moves from the blue spectral range for 0 V to the green range for –1.5 V and to the red range for -5 V. It becomes evident that for –1.5 V the detector is blue and green sensitive and for -5 V blue, green and red sensitive. This behavior is attributed to the device structure where for higher voltages the upper regions remain active.

However, the three spectral responses are linearly independent, and a simple linear color correction can be employed for generating three slightly overlapping responses.

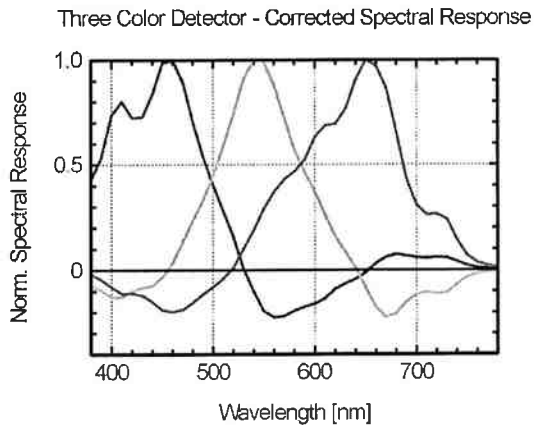

Fig. 5 Corrected spectral sensitivity of CAESAR detector

Fig. 5 shows the corrected spectral sensitivity which has been fitted to the EBU Observer Color Matching Functions. Equation 1 defines the relation between measured (R,G,B) and corrected (R_C,G_C,B_C) color triples.

$$\begin{pmatrix} R_C \\ G_C \\ B_C \end{pmatrix} = \begin{pmatrix} r_r & r_g & r_b \\ g_r & g_g & g_b \\ b_r & b_g & b_b \end{pmatrix} \cdot \begin{pmatrix} R - R_O \\ G - G_O \\ B - B_O \end{pmatrix} \qquad (1)$$

The correction consisting of a 3x3 matrix plus a color offset triple (R_O,G_O,B_O) is obtained using numerical fitting algorithms driven by original and measured color table data.

Sensor Design

The timing diagram of the CAESAR array in Fig. 7 covers two frames. All pixel rows share a common exposure cycle, starting with the pixel reset. During a waiting period the detectors are switched to blue sensitivity through their common front electrode. Blue is the first color to be evaluated in each frame, because switching the detector to short-circuit condition exhibits a slow transient behavior. The blue signal values are stored inside the pixels without intermediate readout operation, whereupon the detectors are switched to green and finally to red sensitivity. The complete exposure cycle covers less than 1 ms, therefore allowing the use of flashlight illumination. All three stored signal values are read out simultaneously in a row-wise mode (see Fig. 6). The CAESAR chip design includes CDS (Correlated Double Sampling) and DDS (Double Delta Sampling) for each color signal to suppress pixel-to-pixel and column-to-column fixed pattern noise, respectively [3]. Direct readout of the signals is possible as well.

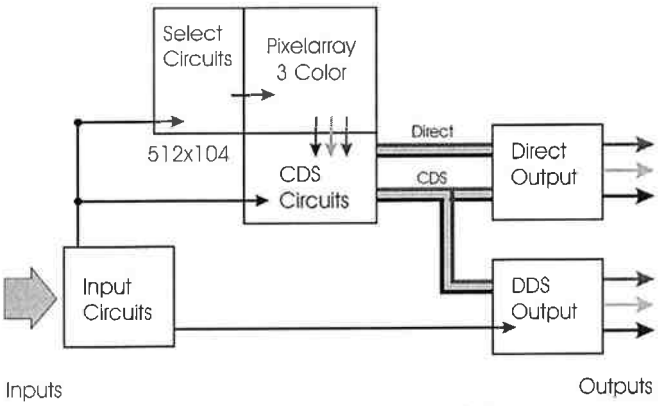

Fig. 6 Block diagram of CAESAR chip

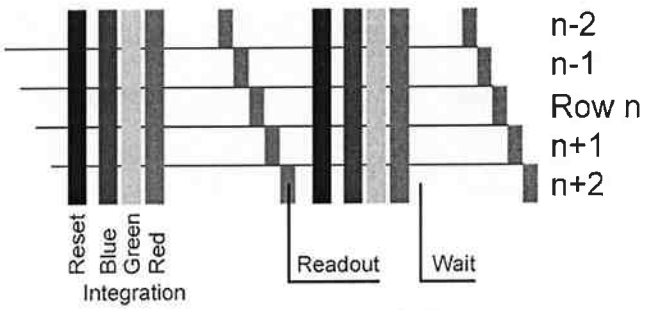

Fig. 7 Timing diagram of CAESAR array

The pixel (Fig. 8) consists of an inverter plus precision capacitor for I/U conversion of the photocurrent, a multiplexer for the red, green and blue signals and three switched source followers as combined storage/driver circuits. According to the timing diagram, Reset is applied globally to the array, whereupon the three Read signals are successively activated, while the Int clock is enabled. Int is disabled for the pixel readout, in order to avoid further integration.

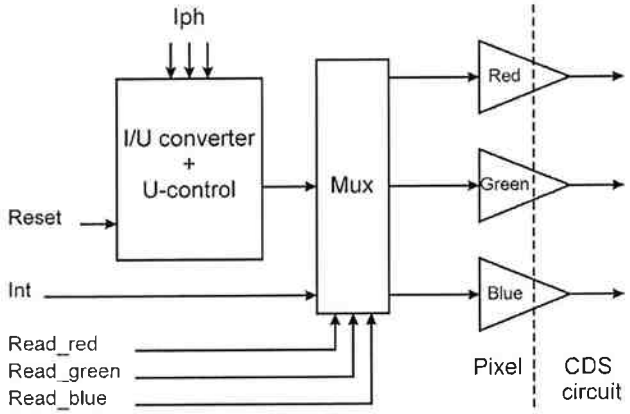

Fig. 8 Block diagram of CAESAR pixel

The functionality was implemented in a double metal double poly 0.8 µm CMOS process. The pixel area is 35 µm × 33 µm. Each pixel contains 16 transistors and one precision capacitor. While the precision capacitor is necessary for storing and converting photo current, simple MOS gates are used to store the voltage representation of color image information.

Fig. 9 depicts the layout of one CAESAR pixel. The TF-via in the middle taps the photo current of the overlaying a-Si:H pin diode and passes it onto the integration capacitance. This is realized in poly1-poly2 for best matching between pixels and can be seen in the middle right of the pixel. The I/U converter output voltage is switched and stored via the switching matrix under the TF-via to the red, green or blue output stages in the left.

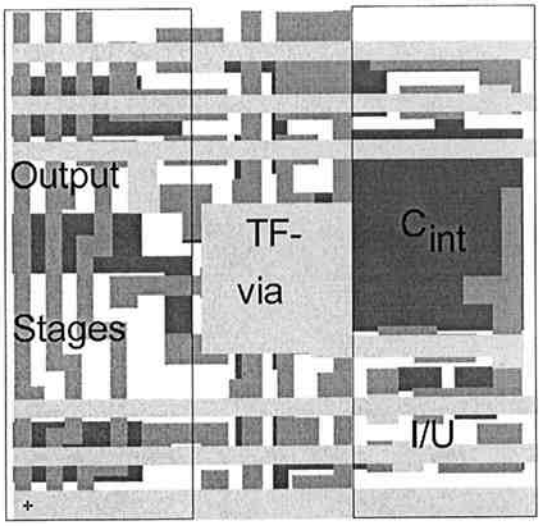

Fig. 9 Pixel layout CAESAR

Fig. 10 shows the chip layout of the CAESAR imager. Beside the active area with row drivers on the left and column CDS readouts on the bottom it contains pad drivers with and without DDS functionality, some digital control functions and several thin film and ASIC test structures inside the pad ring. The addressing of the rows and columns is realized with hierarchical matrix decoders to allow random access while limiting the number and length of addressing lines. The fabricated CAESAR array consists of 512 × 104 pixels, the overall chip size including test circuits is 19.2 mm × 13.8 mm.

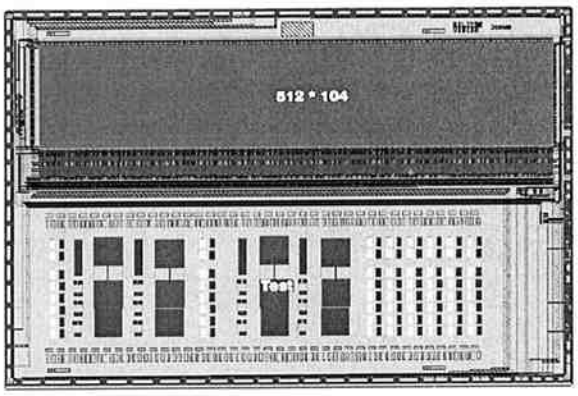

Fig. 10 Chip layout CAESAR

To simplify testing and image capture a camera board has been developed. The board contains all support circuitry including timing generation, supply and reference regulators and a simple analog color correction unit. Image data can be obtained either via a RGB video interface or via three 14 bit AD converters running at 10Msamples. Digital data flow and mode control is handled via a µController board from a software interface on a standard PC.

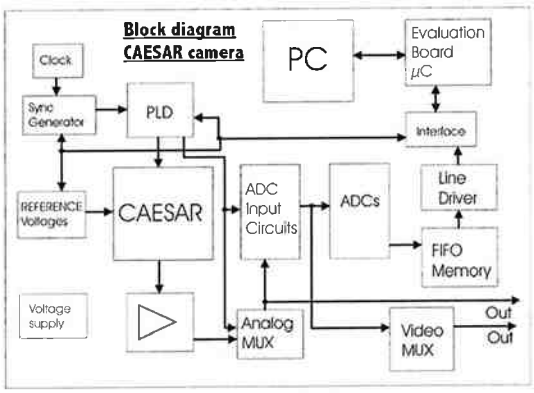

Fig. 11 Block diagram CAESAR camera

Fig. 12 depicts a part of the CAESAR camera board with the CAESAR sensor mounted packaged in a PGA 100 housing. The board uses six connection layers and is assembled in SMD technique mainly. On the left side the Lattice PLD containing the control logic including pattern generation is visible, while on the right side three digital potentiometer can be seen. The potentiometer are used to control the reference voltages. Both the potentiometer and the PLD can be programmed via PC.

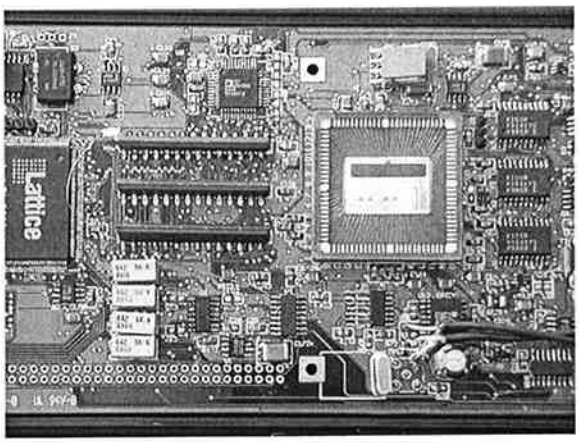

Fig. 12 Camera Board with CAESAR in PGA package

Results

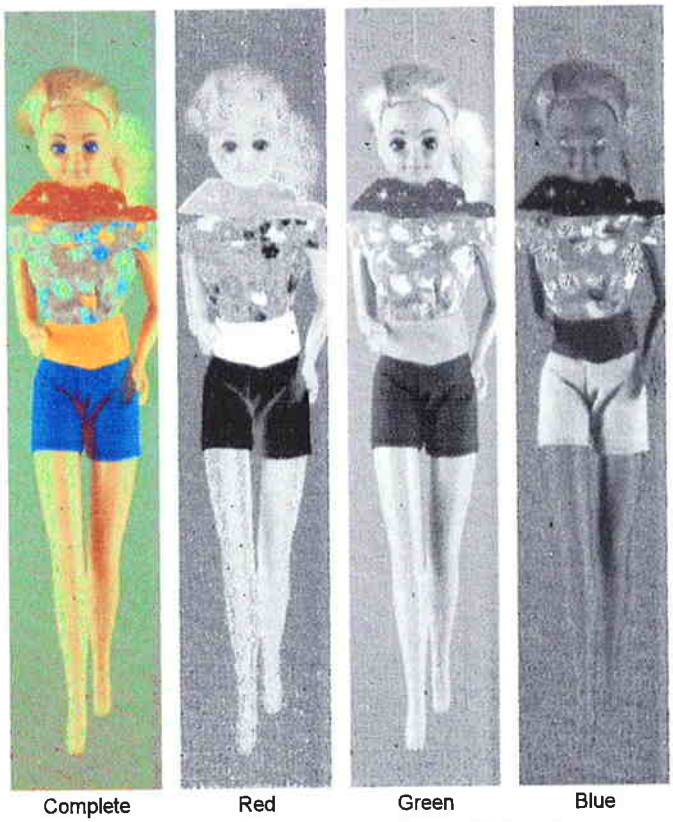

Fig. 13 Color corrected image taken with CAESAR and according color extractions

Fig. 13 shows an image taken with the presented CAESAR array along with the according red, green and blue extractions. It is taken on wafer level on a mixed signal test system with probe station and additional optical extensions. Using the probe station microscope system and a xenon arc light source, a slide containing the original image is projected on the sensor chip. Due to a low illumination level of 400 lux the integration time has been enlarged above the 1ms flash cycle. Actually the image was taken with a 300µs, 400µs respectively 1.5ms R,G,B integration period. After dark level and illumination correction the image has been color corrected as described above.

Fig. 14 depicts a standard color characterization table scanned with a film scanner, the raw signal from the CAESAR imager and the color corrected CAESAR table. While most of the test colors can be reproduced properly some single ones reveal the limitations of CAESAR imagers thin film detector in the present version. TF01,02 and 08 show a reduced red sensitivity of the sensor, while the gray scale pattern TF16 and TF17 expose an illumination dependant shift of color sensitivity. Still being in the first step of developement both color correction and the color diode system will have to be further improved.

Besides, the CAESAR has been tested within the presented camera board. With outdoor illumination conditions video images with a R,G,B integration cycle of less than 1ms have been taken. In video mode readout speeds higher than 11 MPixel/s (direct readout) have been evaluated. With DDS enabled a readout speed of more than 6 MPixel/s is expected.

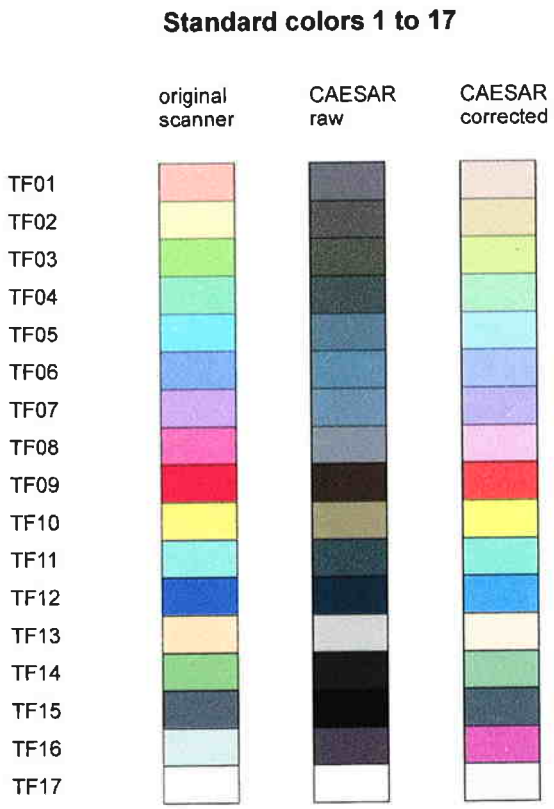

Fig. 14 Original, measured and corrected color table

Conclusion

A sensor array with three color recognition in one pixel has been demonstrated for the first time. This breakthrough was made possible by the versatility of TFA technology and optimization of a-Si:H thin film detectors. A short exposure time of only 1 ms, allowing single shot flash illumination, is accomplished by successively integrating all three color signals without intermediate readout. The prototype being fabricated in a 0.8 µm process, the pixel size is relatively large, still, recent advances in ASIC technologies allow smaller pixels for a marketable product with high resolution.

References

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