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A Page Width CMOS Image Sensor Array

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Background:
Document scanners using conventional image sensor arrays and reduction optics need high illumination levels for high scanning speeds. This problem gets further compounded for color scanners, where only part of the illuminator spectrum is detectable by each color photosite. Using page width image sensor arrays, the illumination requirements can be reduced by orders of magnitude. Also, because of the large pixel size and 1:1 optics using gradient index lenses, one can avoid diffraction-limited performance and off –axis effects.

The Image Sensor Array:
A 12.4"color image sensor array with 400 samples per inch resolution and consisting of 20 chips placed end-to-end colinearly has been developed. Figure 1 shows a diagram of the image sensor array. The chips are placed very precisely in both X and Y directions. A precision dicing process was developed to enable cuts very close to the active circuits without any damage to them. The substrate material was selected to minimize the difference in coefficient of expansion so that periodicity errors at chip boundaries could be maintained in a narrow range over the entire temperature range.

Chip Design:
A key requirement for this design was to obtain a high signal-to-noise ratio for a given irradiance at the image sensor plane. This was the primary reason for going to a 1X imaging system and using a number of co-linearly placed chips. Use of multiple chips to build a single sensor array meant that any non-linearity differences between chips had to be minimized since they show up easily in a scanned image. This placed the additional requirement on the sensor chips to have a highly linear photo-response. This, in turn, led to the use of bias charge on the photodiodes so that high transfer efficiency could be obtained using MOS transistors, and non-linearity related to charge transfer inefficiency could be eliminated. Another requirement was to minimize the periodicity errors in the photodiode pitch across chip boundaries. This required placement of active circuitry within microns of the chip boundary.

A block diagram of the chip is shown in Figure 2. It consists of 3 rows of photodiodes which are coated with red, green, and blue color filters respectively. Each group of three photodiodes shares an amplifier and a shift register stage. The amplifier outputs are brought out on ODD and EVEN video lines to enable high speed operation. The two video lines feed into DC restore and S/H circuits. The outputs of the S/H circuits are multiplexed and fed into the output buffer amplifier.

A schematic of the pixel cell is shown in Figure 3. The red, green and blue photodiodes, PD_R, PD_G and PD_B of each group of 3 diodes, are connected to a bias charge injection transistor T_3 via transfer gates T_{1R}, T_{1G} and T_{1B} respectively. The bias charge injection transistor is used to inject the bias charge into the photodiodes. It enables a high transfer

efficiency when the photo-generated charge is transferred from the large photodiode capacitance to the small reset node capacitance via transfer gates $T_{1(R,\ G\ or\ B)}$ and T_2. Transistor T_4 is used to reset the amplifier inputs.

The timing diagram is shown in Figure 4. There are four parts of the timing sequence, viz. a) reset, b) charge transfer, c) bias charge injection, and d) integration of the photo-current. As shown in the timing diagram, fill and spill technique is used to reset the intermediate node, N1, using both ϕ_R and ϕ_{T2} pulses. This is followed by reset of the pixel amplifier input. After that one of the three T_1 gates, and the T_2 gate are turned on to transfer the charge from a particular row of photodiodes to the amplifier inputs. As shown in the timing diagram, a bias charge is injected into the same row of photodiodes using pulses $\phi_{T1(R,\ G\ or\ B)}$, ϕ_{FZ} and V_{FZ}. to prepare the row of photodiodes for integration of the photo-current. Again, the fill and spill technique is used to make the bias charge voltage independent of threshold variations. The shift register enables multiplexing of the odd amplifier outputs sequentially to the odd video line, and the even amplifier outputs to the even video line. As indicated in Figure 4, the integration of the photo-charge starts after completion of the bias charge injection and ends with the completion of charge transfer.

Performance:
The chip described above enables Electronic Shuttering, Independently Controllable Integration Times for the three colors, and Asynchronous Operation. Performance of the chip is shown in the Table below. It has a noise equivalent exposure of 8.3 pJ/cm^2. The spectral response is shown in Fig. 5. A comparison of irradiance requirements using reduction optics and 1X optics is shown in Figure 6. As can be seen the irradiance requirement with a 1X imaging systems using a page width sensor can be more than an order of magnitude lower than a system using reduction optics and a 7 μm pitch sensor array.

Responsivity	450 nm 550 nm 650 nm	95 133 202	V/μJ/cm^2
Speed	Bar Chip	22 440	MPx/sec.
Dark Noise		1.1	mV
Noise Equivalent Exposure		8.3	pJ/cm^2
Image lag		0	
Photo-response Non-Linearity		<0.5	%
Photo-response Non-uniformity		±10	%

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Reference: A Multichip Page Size Image Sensor, A. Perregaux, Proceedings of the 1998 International Conference on Multichip Modules and High Density Packaging, pp. 516 – 519, April 1998.

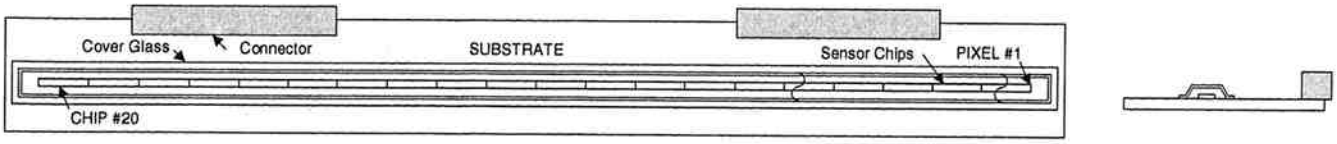

Figure 1: Page Width Image Sensor Array

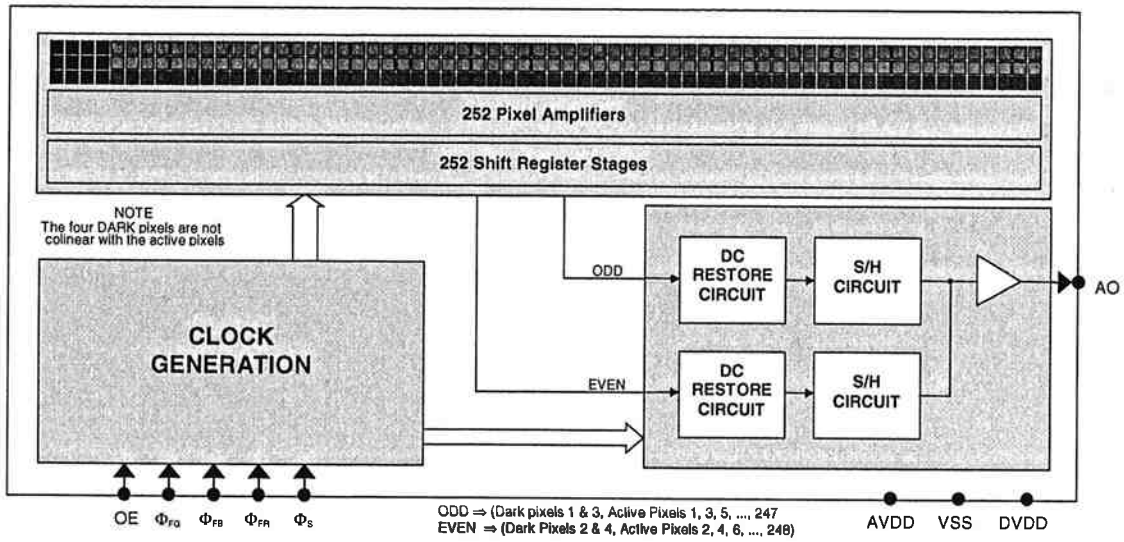

Figure 2: Image Sensor Chip Block Diagram

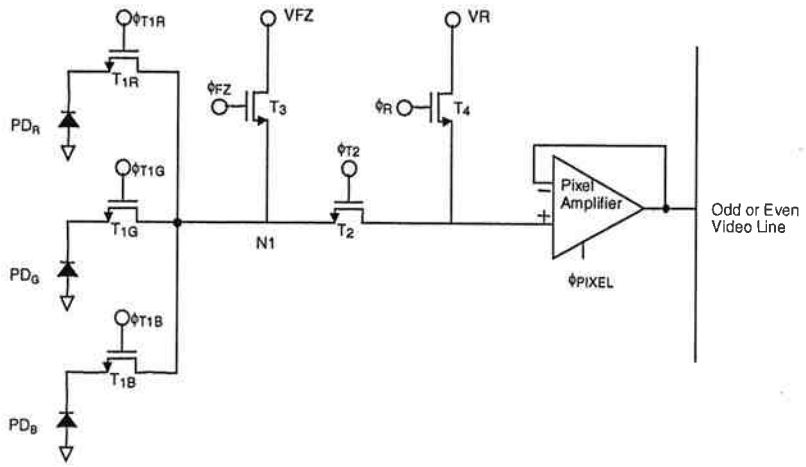

Figure 3: Pixel Cell Showing Photodiodes, Transfer and Reset devices and Pixel Amplifier

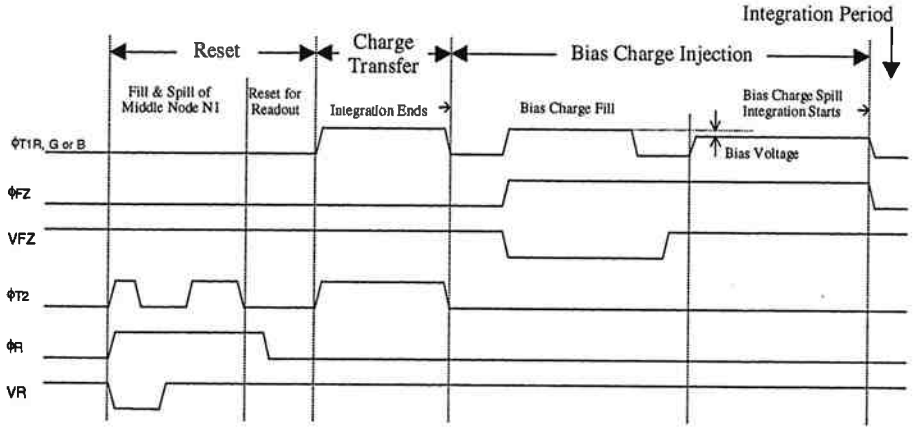

Figure 4: Timing Diagram

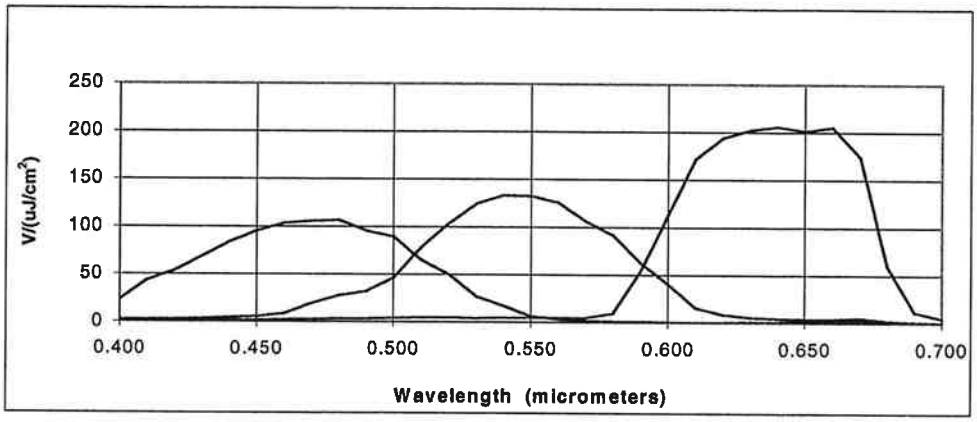

Figure 5: Image Sensor Spectral Response

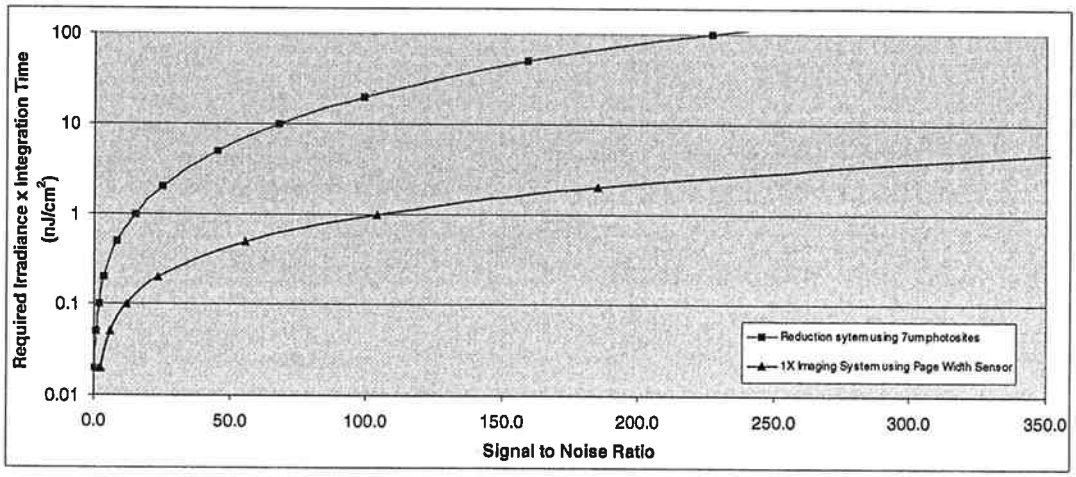

Figure 6: Comparison of Irradiance Requirements with Reduction Optics and 1X Imaging Systems