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An 8M-CCD for an Ultra High Definition TV Camera

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ABSTRACT

A CCD image sensor has been designed and fabricated for an ultra high definition TV camera. With 8 million (4046H x 2048V) pixels and 60 frames/second, this sensor doubles the horizontal resolution, vertical resolution and frame rate of a 2M-HDTV sensor. The high frame rate and large die size posed several technical challenges for sensor design. This paper describes the sensor design, discusses these technical challenges and presents preliminary sensor performance data.

1. Introduction

The spatial resolution of 35mm and 60mm film still exceeds that of high definition TV image sensors. The resolution has been surpassed by some low frame rate [1] or still photography [2] image sensors; however, the increased pixel count poses numerous challenges for moving pictures. A multi-sensor approach, spatially offsetting 2 HDTV sensors, has achieved 1500 TV lines [3]. A single chip image solution doubling the horizontal resolution, vertical resolution and frame rate of a 2M HDTV sensor was the objective of this project. This paper described the sensor and the primary design challenges and includes some preliminary test results.

2. Sensor Architecture

A schematic diagram of the image sensor architecture is illustrated in Figure 1. The split frame transfer design has two 4096H x 1028V storage regions. The sixteen outputs operate at 37.125MHz video rate for HDTV compatibility and utilize 160MHz bandwidth amplifiers for correlated double sampling noise reduction. There are 50 dark pixel columns on the left side. The sensor has been fabricated on a 0.8μm 3-poly 2-metal n-substrate CCD process. Narrow tungsten busses route clock signals and the channel stop bias through the image and storage VCCDs. Tungsten-polysilicon contacts are made over alternate channel stops; the polysilicon is patterned to boost blue light sensitivity especially from 400nm-440nm. A pixel diagram is illustrated in Figure 2. Pixel fill factor is 89%. A vertical overflow drain provides blooming suppression.

Figure 3 is a photograph of the finished sensor. The 2.3" x 2.6" ceramic 150 pin PGA fits a standard 25 x 22 PGA socket. Fast drive capability demanded that each VCCD and HCCD clock be split between 4 pins to limit capacitance. The evaluation electronics generates 37.125MHz 5V HCCD clocks and 1MHz 10V VCCD clocks. The 4-phase HCCD clocks operate in pseudo-2-phase mode for improved video settling.

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3. Frame Rate Design Considerations

RC clock delay analyses identified the 0.5μs HDTV horizontal retrace time as the most demanding timing specification for frame transfer architectures. RC delays scale with the square of the image area width, and a 0.5μs VCCD-to-HCCD transfer becomes quite problematical. The split frame transfer architecture has simultaneous top and bottom VCCD-to-HCCD transfers; consequently a 1.0μs VCCD-to-HCCD transfer is sufficient. This 1.0μs transfer time is achieved through cross connecting all VCCD tungsten busses to low resistance aluminum busses over the storage regions. A non-conducting opaque layer provides storage region light shielding.

4. Die Size Design Considerations

The large die size posed special problems as it was greater than the lithographic stepper field size. The limitation was overcome by a process called stitching [4]. The die pattern for the 8M CCD is partitioned into 12 smaller unique patterns, identified in Figure 4 as A1, A2, B1, B2, C1, C2, D, E, F, G, H, I. These reticle blocks can be placed on 1 or 2 reticles depending on the layer. A sequence of 20 lithographic stepper exposures then reproduce the entire die pattern on the wafer. Mask registration errors and optical artifacts introduce a small (less than 1%) PRNU at the stitch boundaries. One benefit of stitching is that other architectures can be fabricated with the same reticle set, for example 1024H x 2048V, 3072H x 2048V and 8192H x 2048V.

5. Device Parameters and Conclusions

Device characterization is at a very preliminary stage. Testing has demonstrated the 37.125MHz data rate, 60 frames/second, horizontal retrace time, vertical retrace time compliance targets. The measured conversion efficiency is 8μV/*e* and the vertical charge transfer efficiency is greater than 0.99999. Table I lists these measured parameters and other predicted parameter values yet to be tested. Figure 5 illustrates a complete image frame from one sensor. A detail view of the bar target demonstrates that Nyquist resolution has been achieved.

In conclusion we have designed, fabricated and verified functionality of an 8M-CCD image sensor at 60 frames/second. The device is applicable to very high resolution moving picture video systems.

6. References

[1] S. G. Chamberlain *et. al., A 26.2 Million Pixel CCD Image Sensor,* Proceedings of the SPIE, Vol. 1990, pp. 181-191, 1993.

[2] M. Konishi *et.al., Review on Digital Still Cameras,* IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors, Bruges, June 1997.

[3] K. Mitani *et. al., An Experimental 2K x 2K Color Video Pickup System Based on CMD Imagers,* IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors, Bruges, June 1997.

[4] M. Farrier *et. al., Design and Processing Aspects of a 50 Megapixel full Frame CCD image sensor,* IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors, Bruges, June 1997.

Figure 1: Sensor Architecture

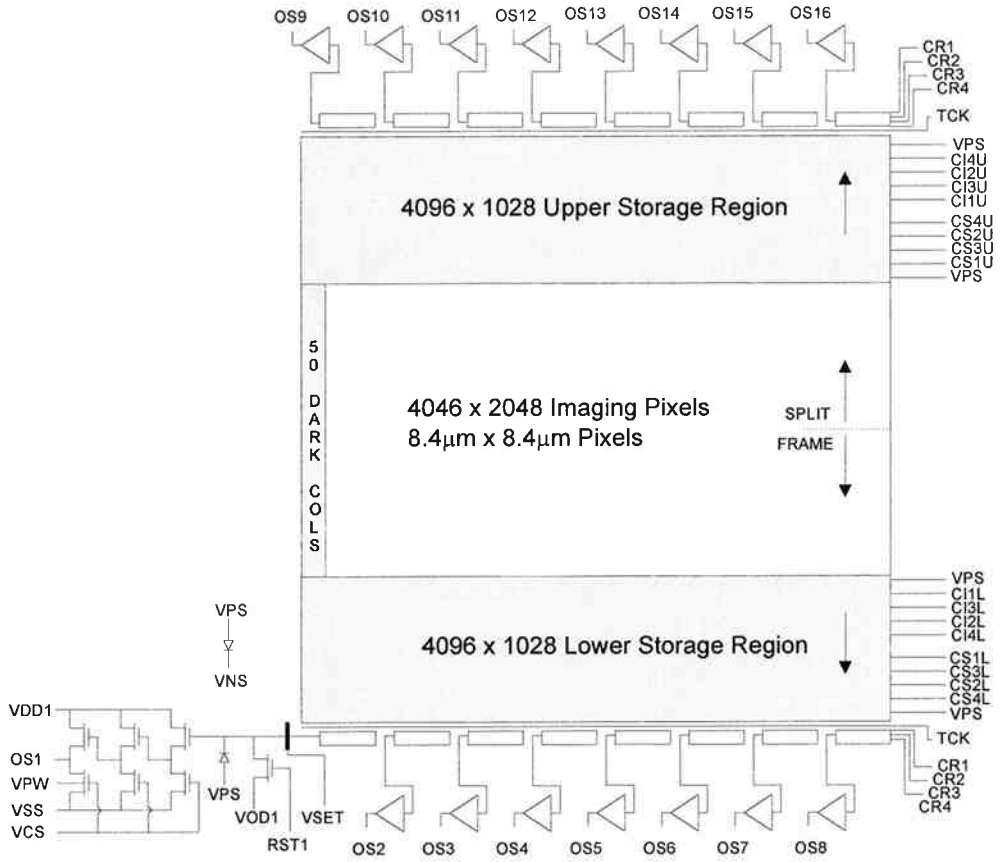

Figure 2: Image Pixel VCCD

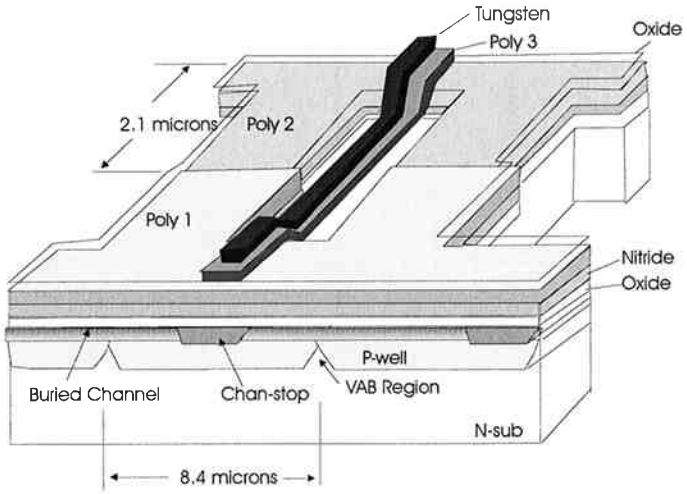

Figure 3: Finished Sensor

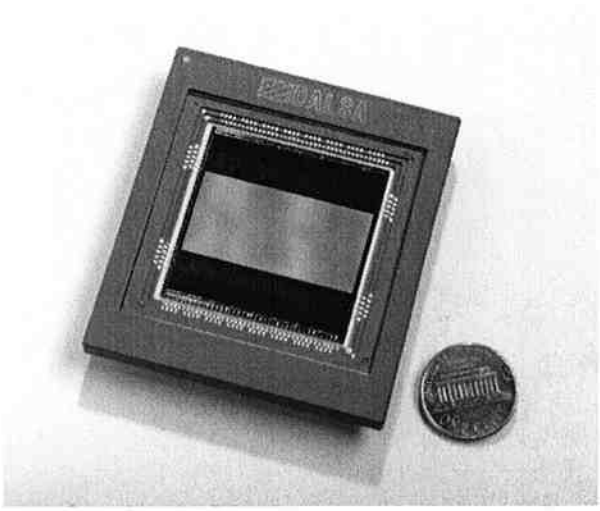

Figure 4 – Photolithography stepping pattern
for one layer of CCD Die

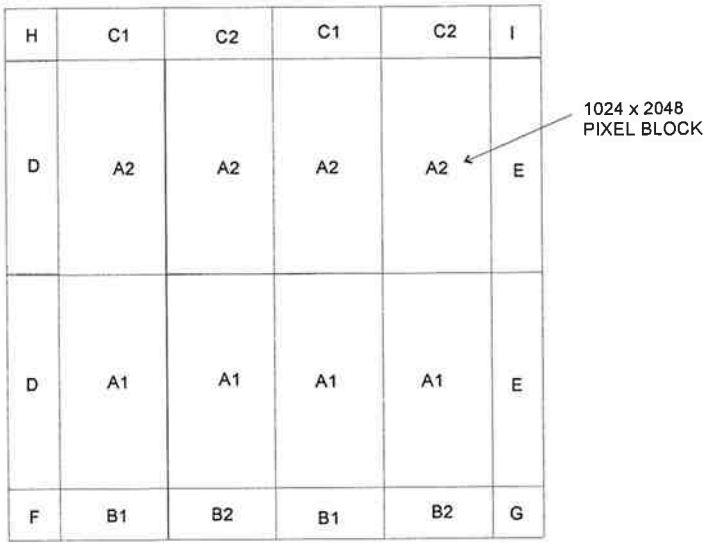

Table I: CCD Sensor Performance

Parameter	Value
Frame Rate	60 fps
Amplifier bandwidth	160 MHz
Image-to-Storage Transfer Time	1.45 ms
Parallel-to-Serial Transfer Time	1 μs
Fill Factor	89%
Responsivity	27.6 mV/lux
QSAT	60,000 e-
Dynamic Range	2000:1

Figure 5 – Resolution Imagery of the 8M-CCD Image Sensor