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Performance Characteristics of a 9216 x 9216 pixel CCD

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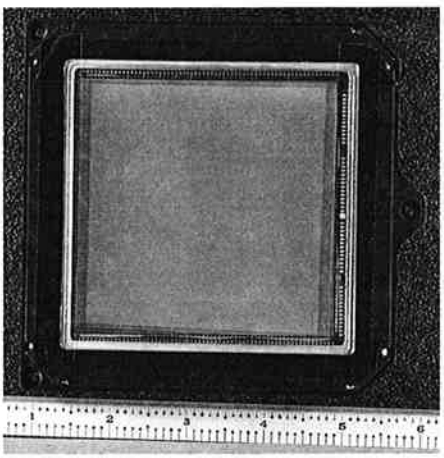
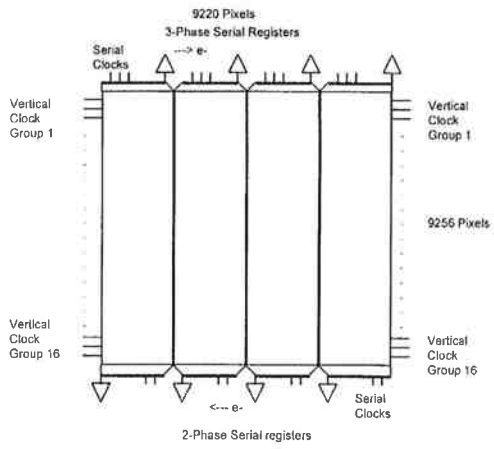
ABSTRACT

Progress made in the past few years in the development of large area scientific imaging arrays has been very rapid. CCD imaging arrays from 3cm x 3cm (2048 x 2048 pixels) to 8cm x 8cm (9216 x 9216 pixels) are available. An ultra high resolution CCD detector array comprised of 9216 x 9216 pixels is discussed. The detector array measures 8 x 8 centimeters and has been scaled to be fabricated in one piece on a 5 inch diameter silicon wafer. Pixel size is 8.75 x 8.75 microns which gives 57 lp/mm resolution. The detector array features a two frame per second readout capability, allowing for collection of video imagery comparable to film. The high geometric accuracy of pixel placement on the array yields a camera suitable for mapping, reconnaissance, space and astronomy applications. In this paper, measured detector array performance, CTE, quantum efficiency, conversion gain, and dark current are presented. Output configuration and design/system tradeoffs will also be described.



9K Detector array in cooled package



9K CCD architecture

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1.0 Introduction

Lockheed Martin Fairchild Systems is currently engaged in volume production of large area charge coupled devices for commercial and scientific applications including 4096 x 4096 imaging sensors with exceptional performance. This paper describes a new 9216 x 9216 CCD imager recently developed at Lockheed Martin. The imager, designed specifically for reconnaissance applications, features close to 85 million active pixels. The pixel size was selected to be 8.75 x 8.75 µm to deliver 57 lp/mm resolution capability. The device measures 80.6 x 80.6 mm and occupies a full 125 mm wafer (Figure1). Designed to replace existing film-based reconnaissance cameras, a single frame occupies over 169 million bytes at 12-bit resolution. The ultra high resolution sensor has been successfully integrated in a framing camera capable of 2 frame per second readout rate.

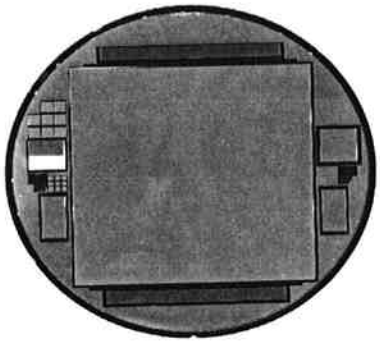

Figure1. 5-inch wafer containing monolithic 9216 x 9216 CCD

2.0 Design & Architecture

The device was designed with 1.5 µm design rules and fabricated with our optimized 3-poly, single metal process and utilizes thin oxide channel stops to maximize the CCD charge handling capacity. The pixel architecture is 8.75 x 8.75 µm with 100% fill factor (Figure 2). Figure 3 shows the configuration of the array. The imaging area is divided into four separate sections, each with an output on top and bottom. The bottom serial registers are two phase, while the top serial registers are three phase. This approach was used to provide redundancy if the yield for the 2-phase serial registers was not adequate. Two phase serial registers require very simple clocking for high speed operation, but are somewhat more complex in design layout. Fortunately, we did not encounter any performance issues with the 2-phase registers. To

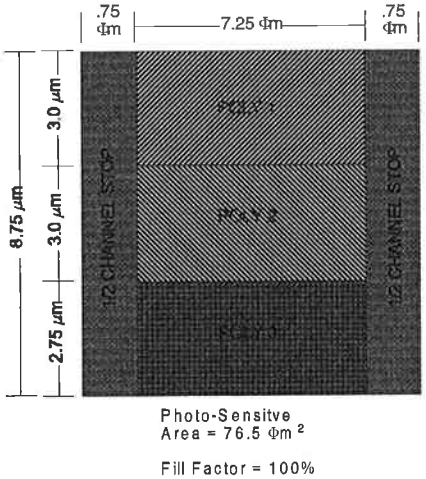

Figure 2 Pixel Layout

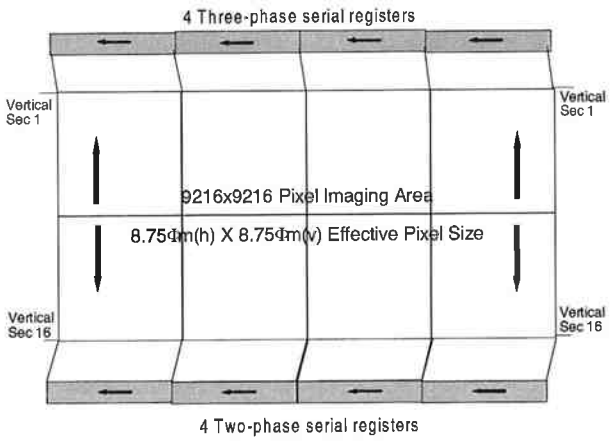

Figure 3 Imager Architecture

minimize peak vertical array clock currents, the image array is partitioned into 16 sections of three phases. This substantially reduces the capacity each external clock driver is required to drive. A three stage source follower terminates

each serial register for high speed operation.

3.0 Performance

The performance of these arrays has met or exceeded our design parameters. A detailed listing of design goals and measured results are shown in Table 1. Image quality is excellent (Figure 4) and readout noise performance is less than 25 electrons rms at 25 Mpixels/second readout rate. When clocked at 100Khz at –40 Deg.C noise is under 7 electrons making the array suitable for scientific applications. At 200 Khz the noise is less than 9 electrons. Present camera output rate has reached 2 frame per second. At a 50 Mhz readout rate it should be possible to achieve better than 2 fps.

Table 1. 9K x 9K CCD Imager Technical Specifications & Performance

Parameter	*Design Goals*	*Measured Results*
Frame Size	81mm x 81 mm	As Designed
Image Elements	9216 x 9216	As Designed
Pixel Size	8.75 x 8.75 µm	As Designed
Architecture	Full Frame	As Designed
Operating Modes	Framing/Image Motion Comp.	As Designed
No. Vertical Bus Taps	16/side	As Designed
Number of Outputs	4	8(4 Three Phase/ 4 Two Phase)
Output Type	3-Stage Buried Channel	As Designed
Integration Time	0.5 ms to 10.0 ms	As Designed
Frame Rate	1 Frame/Sec	> 1 Frame/Sec
Pixel Full Well	> 70,000 e-	>100,000 e-
Vertical CTE	> 0.999995	> 0.999999
Horizontal CTE	> 0.999995	> 0.999995
Dark Current / non-MPP	≤ 120 pA/cm^2	< 70 pA/cm^2
Pixel Readout Rate	> 25 Mhz	> 40 Mhz
Readout Noise @ 25 Mhz	< 40 e- rms	< 25 e- rms
Conversion Gain	≥ 5 µV/e-	≥ 9 µV/e-
Operating Temperature	< 15 Deg. C	< -70 Deg. C
PRNU	≤ 5% Vsat	< 5 % rms
DSNU	≤ 1 mV	< 1 mv rms
Quantum Efficiency	≥ 35% -(0.55 nm – 0.8 nm)	≥ 30%
MTF @ Nyquist	≥50%	≥ 50%
Vertical Transfer Time	≤ 92.4 µsec	< 92 usec
Array Transfer Gate Time	≤ 10 µsec	< 10 usec

The array is driven by 16 groups of 3-phase vertical clocks to reduce the capacitance that each external clock driver is required to drive. The 16 vertical clock sets can be driven in parallel. The horizontal registers at the top and bottom of the detector array are divided into four parts. There are a total of 8 output taps from the array. Each output amplifier can be operated at up to 40 MHz. Currently, the clocks operate at 25 MHz producing a data output rate of 200 million pixels per second.

High Charge Transfer Efficiency (CTE) was achieved, particularly in the vertical direction. In a 3-phase structure of the vertical register, three shifts are required to move the charge each pixel. Transferring charge from the top of the array to the bottom and into the horizontal register requires 9,216 x 3 or 27,648 shifts. Vertical charge transfer efficiency has been measured to be 99.9999%. The horizontal CTE was measured to be 99.995%. Horizontal CTE is less critical since the readout arrangement effectively reduces the number of transfers to a quarter of the number of vertical transfers.

4.0 Conclusion

As semiconductor fabrication technology continues to improve, larger wafer sizes will allow ultra large area charge coupled devices to be developed to replace film technology for many critical applications. The use of these high performance CCDs will continue to expand rapidly as manufacturing costs are reduced and system speed and resolution capabilities are optimized.

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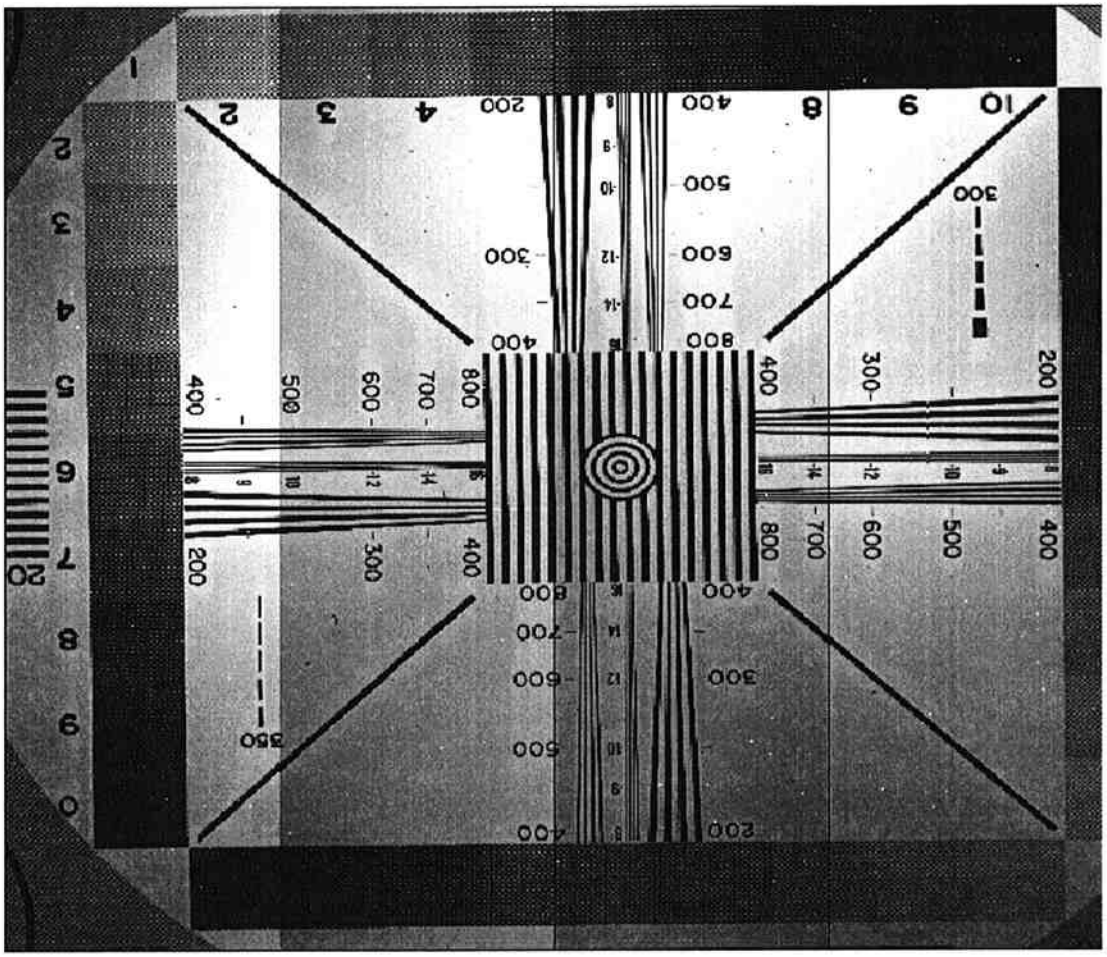

Figure 4 Uncorrected image produced with Lockheed Martin 9216 x 9216 CCD of a resolution target projected through a 35 mm lens.