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A Partially Overlapped X-ray Imaging Pixel with Low Leakage and High Sensitivity

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ABSTRACT

This paper compares various pixel configurations for large area x-ray imaging applications. The pixel comprises a molybdenum based amorphous silicon (Mo/a-Si:H) Schottky diode as an x-ray detector and an a-Si:H thin film transistor (TFT) as a switch. The TFT used in this application has been optimized for low leakage current (~10fA) [1]. A detailed discussion of pixel configurations in terms of process issues (mask count and film stress) and performance issues (leakage current and x-ray sensitivity) will be presented.

INTRODUCTION

X-ray imaging has wide spread applications in medical imaging and non-destructive testing of materials. Amorphous silicon is a good candidate material for digital x-ray imaging due to its large-area capability, good photosensitivity, resistance against radiation and low cost [2].

Recently, we reported a direct x-ray detection scheme based on Mo/a-Si:H Schottky diode [3]. In this diode, which is optimized for low energy x-rays, the interaction of x-ray photons with Mo atoms leads to injection of high energy electrons, by virtue of the photoelectric effect, into a reverse-biased a-Si:H depletion layer, where electron multiplication yields a gain. This diode operates at low reverse bias (< 4V) and yields an x-ray sensitivity of 10^8 electrons over x-ray source voltage range of 40-100 kVp.

The advantages of using this Schottky diode as a low energy x-ray detector over other x-ray detection schemes are that 1) it does not require an intermediate scintillating (phosphor) layer which converts x-rays into visible light [2], and 2) electrons are easily collected without the need of a high bias voltage [4].

This paper will discuss the issues related to fabrication of different pixel structures along with a comparison of their performance in terms of leakage current and sensitivity. It will also discuss what can be done to further improve pixel performance

EXPERIMENTAL

One of the more difficult design requirements for large-area imaging is a high sensor fill factor. In an attempt to achieve high fill factor, the Schottky diode is stacked on top of the TFT (Figs. 1 & 2), and compared with the conventional pixel structure commonly used in imaging applications (Fig. 3). The fabrication processes of pixels in Figs. 1-3 have been reported in [5]. In all pixels, the detector is 200 μm x 200 μm.

The fully overlapped pixel in Fig. 1 would lead to the highest fill factor. However, since the gate area of the TFT is covered by the bottom electrode metal of the diode, it has a highly conducting back channel and, therefore, the leakage current is found to be very high (~100 nA). Further discussion on the leakage current will be presented later in relation to Fig. 5. The leakage current of the

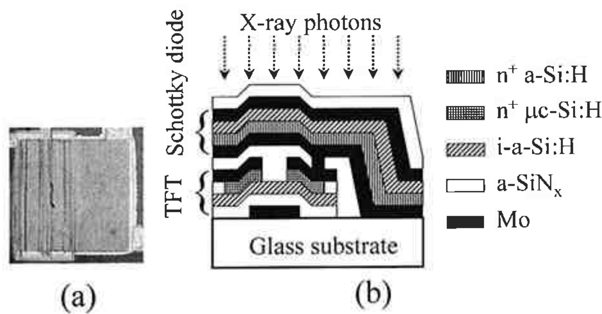

Fig. 1: Fully overlapped x-ray pixel; a) top and b) cross-sectional views.

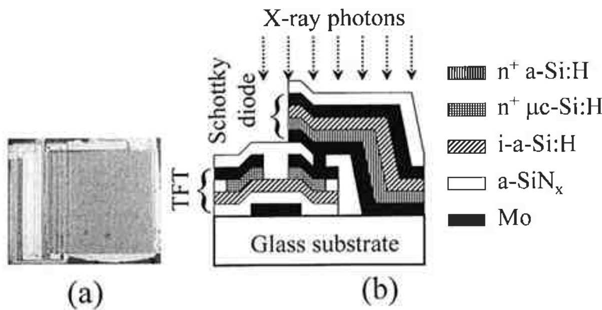

Fig. 2: Partially overlapped x-ray pixel; a) top and b) cross-sectional views.

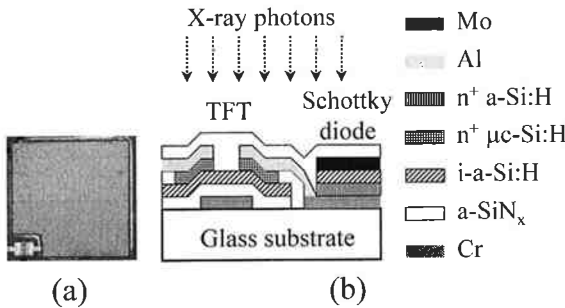

Fig. 3: Non-overlapping x-ray pixel; a) top and b) cross-sectional views.

partially overlapped pixel in Fig. 2 is comparable to the non-overlapping pixel in Fig. 3. But because of the stacking of devices, the partially overlapped pixel process requires 11 masks, whereas the non-overlapping pixel process requires only 7 masks. The geometry of the TFT in the non-overlapping pixel is minimized to be W/L = 20μm/10μm to preserve fill factor. The TFTs in Figs. 1 & 2 are W/L = 200μm/20μm. The deposition conditions for each of the different thin film layers are summarized in Table 1.

Table 1: Deposition conditions of films.

	System	Temp. (°C)	Pressure (mTorr)	Power (W)	Dep. rate (Å/min)
Cr	DC sputtering	25	5	200	112
Mo	DC sputtering	25	5	80	45
Al	DC sputtering	25	10	200	75
a-SiN_x	PECVD	260	400	110	95
i-a-Si	PECVD	260	150	10	110
n^+ a-Si	PECVD	260	150	10	50
n^+ μc-Si	PECVD	260	270	16.7	18

RESULTS & DISCUSSIONS

When devices are stacked on top of each other as shown in Figs. 1 & 2, the intrinsic stress of films becomes an important fabrication issue. In the sensor fabrication, a 500nm Mo layer needs to be deposited on top of a 1μm a-Si:H layer to form the Schottky barrier interface [3]. When a thick Mo layer is deposited on the stacked pixel structure, the layers beneath are unable to withstand the shear stress, thus, causing the films to crack and peel off the substrate [5].

Since the film thickness is much smaller than that of the glass wafer, the mechanical stress induced by the deposited thin film can be approximated by [6];

$$Stress = \frac{d}{R^2}\frac{E_s}{3(1-v)}\frac{T_s^2}{T_f} \quad (1)$$

where, d is the displacement due to the bow, R is the knife edge radius of the instrument, E_s is the Young's modulus for the substrate, v is the Poisson's ratio, T_s is the substrate thickness, and T_f is the film thickness. The measured mechanical stresses of films, deposited on glass substrate under the deposition conditions shown in Table 1, are listed in Table 2. If the interfaces are assumed to be abrupt [6], its shear tolerance can be

estimated to be $5x10^8$ N/m^2. From the values in Table 2, one can easily observe that the interface between Mo and a-Si:H (and/or a-SiN_x) experiences a shear stress which is greater than its assumed tolerance. The intrinsic stress of the Mo film can be reduced by changing its process pressure. In fact, we found that the intrinsic stress of the Mo film when deposited at 3mTorr, as opposed to 5mTorr, is in a compressively stressed state with a magnitude of $1.85x10^8$ N/m^2, which is compatible to that of a-Si:H layer. Additional information on film stress has been reported in [5].

Table 2: Stresses of films deposited on glass.

	Stress (10^8 N/m^2)	State
Cr	5.75	Tensile
Mo	6.03	Tensile
Al	5.03	Compressive
a-SiN_x	1.02	Tensile
i-a-Si	1.16	Compressive
N^+ a-Si	3.05	Compressive
n^+ μc-Si	14.7	Compressive

One important requirement in terms of pixel performance is the leakage current. The leakage current of the sensor (see Fig. 4) in all different pixels is the same regardless of the pixel configuration. However, the same is not true for the TFTs. Fig. 5 shows that the leakage current in the fully overlapped structure is very high compared to the other designs. In the fully overlapped pixel structure, when the TFT gate voltage is negative, the electrons in the a-Si:H experience an electric field forming a steady parasitic back channel at the a-Si:H/aSiN_x interface, hence, providing a high conducting path from drain to source.

The partially overlapped and non-overlapping pixels are exposed to x-rays for

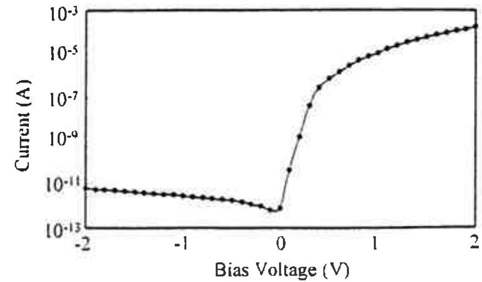

Fig. 4: I-V characteristics of Mo/a-Si:H Schottky diode x-ray detector (200μm)^2.

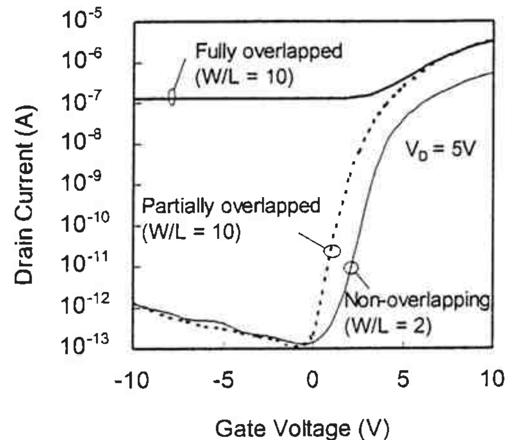

Fig. 5: Leakage currents of TFTs in the different pixel structures.

50ms at various source voltages in the range of 30-120 kVp. The x-ray photons are generated by Mercury Modular X-ray machine with a molybdenum target at an incidence angle of 16 degrees. The x-ray radiation is measured with a RTI Solidose 300 digital Dosimeter whose operating range is from 0.5 μR to 23,000 R. The corresponding x-ray dose is plotted in Fig. 6. The biasing of the pixel and the measurement of the current are carried out with Keithley 236 Source-Measure Units, remotely controlled by a computer via HPIB. The Schottky diode is reverse biased at 1V (see Fig. 7). The drain of the TFT is connected to a Source-Measure Unit for current measurement, and the gate of the TFT is pulsed at low frequency at 1V.

In order to readout the x-ray generated charge, the pixel in Fig. 7 is operated in the following sequence. The Schottky diode is

3. Frame Rate Design Considerations

RC clock delay analyses identified the 0.5μs HDTV horizontal retrace time as the most demanding timing specification for frame transfer architectures. RC delays scale with the square of the image area width, and a 0.5μs VCCD-to-HCCD transfer becomes quite problematical. The split frame transfer architecture has simultaneous top and bottom VCCD-to-HCCD transfers; consequently a 1.0μs VCCD-to-HCCD transfer is sufficient. This 1.0μs transfer time is achieved through cross connecting all VCCD tungsten busses to low resistance aluminum busses over the storage regions. A non-conducting opaque layer provides storage region light shielding.

4. Die Size Design Considerations

The large die size posed special problems as it was greater than the lithographic stepper field size. The limitation was overcome by a process called stitching [4]. The die pattern for the 8M CCD is partitioned into 12 smaller unique patterns, identified in Figure 4 as A1, A2, B1, B2, C1, C2, D, E, F, G, H, I. These reticle blocks can be placed on 1 or 2 reticles depending on the layer. A sequence of 20 lithographic stepper exposures then reproduce the entire die pattern on the wafer. Mask registration errors and optical artifacts introduce a small (less than 1%) PRNU at the stitch boundaries. One benefit of stitching is that other architectures can be fabricated with the same reticle set, for example 1024H x 2048V, 3072H x 2048V and 8192H x 2048V.

5. Device Parameters and Conclusions

Device characterization is at a very preliminary stage. Testing has demonstrated the 37.125MHz data rate, 60 frames/second, horizontal retrace time, vertical retrace time compliance targets. The measured conversion efficiency is 8μV/*e* and the vertical charge transfer efficiency is greater than 0.99999. Table I lists these measured parameters and other predicted parameter values yet to be tested. Figure 5 illustrates a complete image frame from one sensor. A detail view of the bar target demonstrates that Nyquist resolution has been achieved.

In conclusion we have designed, fabricated and verified functionality of an 8M-CCD image sensor at 60 frames/second. The device is applicable to very high resolution moving picture video systems.

6. References

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