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An Improved Digital CMOS Imager

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ABSTRACT

A new 8×8 μm^2 4T nMOS pixel layout with an optically optimized square photodiode (PD) is presented. The 26 % fill factor, square photodiode layout provides significantly improved modulation transfer function (MTF) and permits more efficient microlens structures to increase the pixel effective fill factor. For color imaging applications which use on-chip RGB Bayer pattern color filters, the new pixel layout significantly reduces crosstalk typically found between red-green-red and blue-green-blue pixels. Measured data showing improvements over an earlier rectangular PD structure [1] are presented. A 3.3 V single chip digital CMOS imager with 640 × 480 (VGA) pixel array, parallel bank of 640 pseudo-10b ADCs using a novel double slope conversion technique to expand signal dynamic range, 3.04 kB DRAM line buffer, digital double sampling (DDS) circuitry and digital control block is implemented using a 0.5μm single poly, triple metal DRAM baseline.

1. INTRODUCTION

Unlike CCD imagers, MOS imagers typically have additional transistors integrated within each pixel which must be incorporated in the pixel design while optimizing pixel layout to achieve maximum effective fill factor and sensitivity. Often times, increasing the absolute fill factor of a pixel does not necessarily result in improved sensitivity since the geometric shape of the PD can impact the efficiency of microlenses and optical characteristics of the PD [2],[3]. To maximize the effectiveness of the microlenses, the shape of the photocollection region and topology of neighboring structures are as important as the absolute area of PD.

In this paper, we present a new 8×8 μm^2 4T nMOS pixel structure with optically optimized PD for improved effective fill factor and MTF. Pixel MTF is significantly improved by using hemispherically shaped microlenses which are matched to square photocollection regions. In addition, increased spacing between neighboring PDs resulted in better optical and electrical isolation, higher MTF, and improved color reproduction with reduced fixed pattern noise(FPN).

At low light levels, noise in the pixel output is usually limited by AD converter resolution. At high light levels, pixel output is typically dominated by shot noise and requires large input dynamic range. For most imaging applications, 8b data converter SNR is sufficient for pixel AD conversion at optimum exposure conditions. However, 10b dynamic range is typically required for satisfactory data conversion over the full range of possible exposure conditions. A double slope AD conversion technique is proposed to provide enhanced dynamic range and higher resolution and is suitable for use in a parallel bank ADC architecture and direct integration with the 640 × 480 VGA MOS imaging array. The resolution of a single slope AD converter is simply determined by slope of the analog voltage ramp and clock frequency of the synchronized digital counter and speed of the digital latch. Using an analog ramp generator with a programmable slope and digital counter with variable

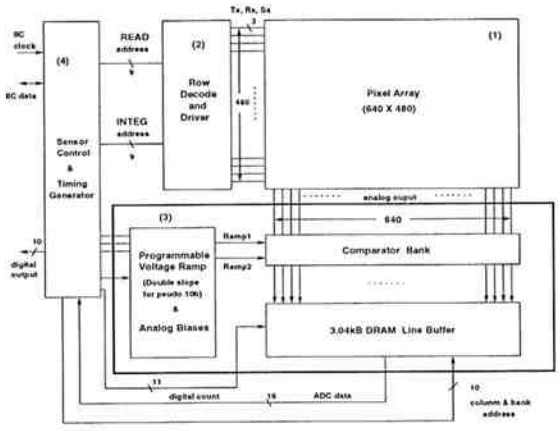


Fig. 1. The block diagram of a digital CMOS imaging system.

increment, the resolution of a single slope AD converter was improved to 10b for low level outputs by using a low slope voltage ramp and was reduced to 8b for large level outputs by using a higher slope voltage ramp and digital increment for an overall 10b dynamic range.

2. 640 × 480 VGA CMOS IMAGER

The CMOS image sensor system consists of 4 sub block ; (1) VGA pixel array, in which each pixel has an optically optimized square sensing region, (2) a bank of 640 row decoders and drivers, (3) a bank of 640 parallel ADCs with 3.04 kB DRAM line buffers and analog subblock, and (4) digital logic for the sensor control and timing generation. This imager is fabricated using 0.5 μm DRAM baseline process with single poly, triple level metal. The 8.7 × 6.9 mm^2 chip requires a single 3.3V power supply and at 12MHz consumes < 55 mW. In Fig. 1, a block diagram of the complete system is shown.

3. PIXEL DESIGN

The basic circuitry of the 8×8 μm^2, 4T nMOS pixel with low voltage PD is shown in Fig. 2. Proper pixel operation requires three separate control signals, Tx, Rx, and Sx [1]. MR is implemented as a depletion mode transistor in order to permit the floating sensing node to be reset to VDD and to reduce Vt dependence of the reset voltage.

Digital Double Sampling (DDS) is used to remove FPN caused by a process variations, device mismatch, and kT/C reset noise. During the programmable integration time, the photo charge collection region is isolated from the sensing node by MT, and the floating node is reset to VDD through MR. After reset, MR is switched off to isolate the floating node, and the initial floating node voltage of the pixel (reference count) is read. After the completion of the integration period, MT is

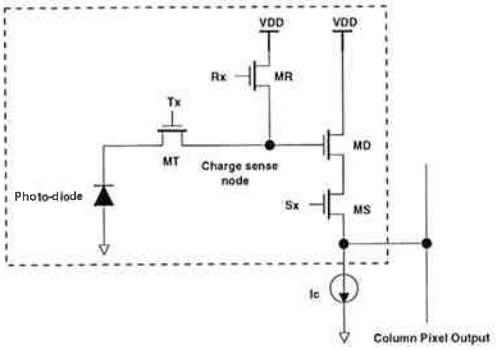


Fig. 2. Equivalent circuit of 4T nMOS pixel.

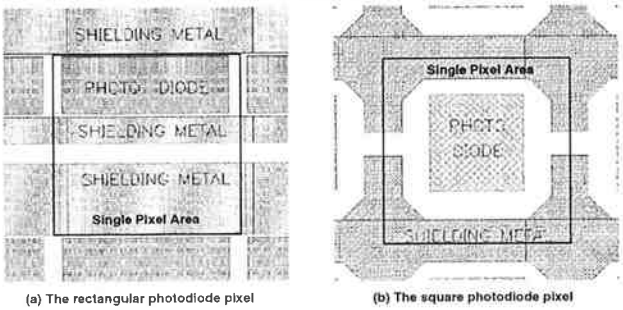


Fig. 3. Photodiode layouts.

toggled by Tx which causes the transfer of collected electrons from the low voltage PD to the sensing node. The resulting change in the floating output voltage (raw data count) is read. The sensitivity of the floating node was designed to be 40 $\sim$ 43 μ V/e$^-$. Overall timing diagram showing typical pixel operation is shown in Fig. 4

3.1. Rectangular PD pixel

An optimized pixel with maximum PD area was previously presented [1] and was shown to have good performance but also had several short comings. In order to maximize fill factor, the shape of the PD was rectangular and is shown in Fig. 3(a).

Pixel-to-pixel cross talk is directly correlated to the spacing of neighboring pixel PDs. Decreased PD spacing results in higher optical cross talk due to photons entering at oblique incident angles or through scattering and the resulting collection of photogenerated charge in a neighboring pixel [6]. Even under fully collimated illimunation, electrical cross talk increases with smaller PD spacing due to the random diffusion of photocharge generated outside of the PD depletion region. For a B/W sensor, image sharpness or MTF is degraded by pixel-to-pixel cross talk. However for a single chip color sensor with color filter array, the resulting cross talk between pixels of different color results in color distortion. In particular, for the rectangular PD with RGB Bayer pattern color filter, a difference of 10% in the response of G_R(green pixels immediately neighboring red pixels) and G_B(green pixels immediately neighboring blue pixels) under uniform illumination with white light was measured. The resulting difference in green pixel responsitivity results in color mosaic noise which is clearly visible using high resolution ADC setting and at high magnification.

Microlens technology can be used extremely effectively by CCD and CMOS image sensors to increase the pixel effective fill factor by using small microlenses formed above the PD of every pixel to collect and refocus photons that would have otherwise been absorbed in nonphotosensitive regions of the pixel. Design of both the microlens structure and PD should be considered when optimizing pixel performance. For the rectangular PD, the a hemicylinderically shaped microlens will provide the optimum increase in effective fill factor. The hemicylinderical lens refocuses illumination in the verticle direction to increase effective fill factor but provides no benefit in the horizontal direction. However, more importantly, pixel-to-pixel cross talk is actually amplified between horizontal neighboring pixels and results in increased color mosaic noise.

Finally, for large area imaging arrays the distribution and routing of power, analog bias voltages, timing signals and analog output voltages is critical for image sensor performance and in particular can account for systematic mismatches in pixel characteristics. To address these issues, an optically optimized pixel and a double slope ADC bank was designed and implemented for improved image quality.

3.2. Square PD Pixel

When microlenses are used, pixel performance can be significantly improved by using a square PD with maximized spacing between neighboring PDs. The larger spacing between neighboring PDs reduces optical and electrical pixel-to-pixel cross talk, improves MTF, and reduces color mosaic noise. In addition, metal layers in the imaging array are not only used for power and signal routing but are also used as a light shield with special attention paid to the optical path and morphology of the microlens structure. In particular, for a centrally located square PD, a hemispherical lens is most efficient. The hemispherical lens permits very high effective fill factor while maintaining low pixel-to-pixel crosstalk. A comparison of the rectangular PD and square PD pixels are shown in Fig 3. The fill factor of rectangular PD is 28.13% and the square PD is 26.25%. The smaller fill factor of the square PD results in slightly lower charge capacity which can easily be adjusted using several techniques [2] [3]. By adjusting the PD doping profiles, square pixel as shown in Fig 3 (b) is expected to provide improved performance through higher optical efficiency and lower cross talk.

4. DOUBLE SLOPE ADC

A double slope technique was implemented to improve the dynamic range and resolution of the single slope ADC bank architecture previously presented [1]. In the single slope ADC bank architecture, a parallel bank of continuous time comparators and digital latches are driven by a voltage ramp generator and a synchronous counter. Parallel AD conversions are performed by latching the digital counter at the time when the analog ramp voltage matches the raw analog pixel values. Offset errors in the comparators and in the pixel are compensated by using digital double sampling (DDS) which digitally subtracts the digital conversions of the initial pixel voltage from the pixel voltage after charge transfer from the photodiode. By using a bank of parallel ADCs to convert raw analog pixel voltages into offset corrected digital output, the speed and power requirements of each individual converter are significantly reduced as demonstrated in both CMOS and CCD/CMOS image sensors [4].

The resolution of the single slope ADC can be simply computed from the step size or slope of the analog ramp voltage and the number of clock cycles in the conversion time. The maximum clock speed is determined by the comparator delay and resolution. Increased ADC resolution requires exponentially increasing the number of clock cycles by using longer AD conversion times or by using higher clock frequencies with associated higher power consumption for high speed comparator and counter operation. In imaging applications, 10b resolution is often needed for low light conditions where pixel noise

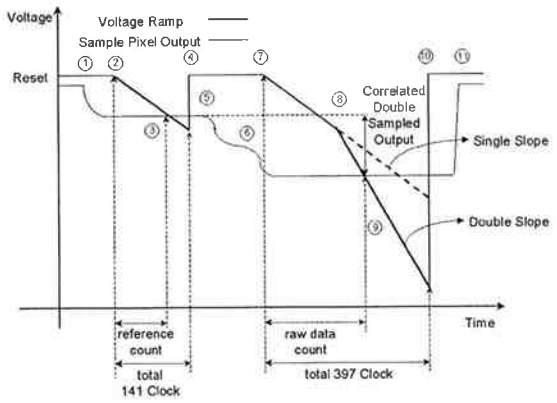


Fig. 4. Typical conversion cycle for a double slope ADC with DDS.

is dominated by quantization in the ADC. However, at high light levels, the pixel output is limited by illumination shot noise such that 8b resolution is usually sufficient. Furthermore, typical image processing applications such as application of gamma correction expand low pixel values and compress high pixel values. Therefore to take advantage of these characteristics, a double slope ADC was implemented which provides high resolution at low pixel values with a shallow slope analog ramp and later switches to high dynamic range at high pixel values with a steep slope analog ramp. Since the analog ramp and digital counter are both synchronized and have programmable step sizes, the converter resolution is enhanced for low pixel values which require fine digital codes. Similarly, the converter dynamic range is enhanced for high pixel values which use coarser digital codes since they are dominated by illumination shot noise by using a programmable double slope ramp generator. Finally, the DDS operation is quite important and provides a type of random 10b dither to prevent quantization artifacts when in the expanded dynamic range of the converter.

Fig 4 illustrates a typical conversion cycle for double slope ADC with DDS. At (1) pixel reset gate swiched off, and resulting output node voltage is converted and stored as reference level (2-4). Photocharge is transferred to sensing node by toggling pixel transfer gate (5-6), and the resulting voltage level is again converted (7-10). However, the double slope technique switches to a steeper slope analog ramp voltage and associated larger counter increment to realize a wider dynamic range within the same number of clock cycles. Change in output voltage is directly proportional to photocharge and is computed by digitally subtracting the two converted data. As seen in Fig 4, the dynamic range is enhanced compared to a simple single slope ADC plotted in dashed line. Using a programmable analog ramp and digital counter increment size, the implemented double slope ADC bank was designed for 10b resolution for the low inputs, 8b SNR for the high level inputs and an overall 10b dynamic range.

5. MEASUREMENTS AND RESULTS

Accurate measurements of 8×8 μm^2 blocks of the rectangular PD pixel and square PD pixel were taken under the same illumination conditions. The results are summarized to Table 1.

The fill factor simply represents the actual area of the PD

Table 1. Summary of Pixel Characteristics

Pixel Type	Rec. PD	Squ. PD
Pixel Size	8×8 μm^2	8×8 μm^2
Fill Factor	28.13 %	26.25 %
Effective Fill Factor	75 %	90 %
Min. Illumination	0.7 lux	0.35 lux
Dynamic Range	25 dB	36 dB
Sensitivity	3.65V/lux·sec	3.8V/lux·sec
G_R G_B crosstalk.	10 %	0 %
Pixel Uniformity	5.9 @ 150	2.3 @ 150
Dark Current	$\sim$ 25 pA/cm^2	$\sim$ 25 pA/cm^2

without consideration of any microlens structure. The effective fill factor is estimated from the size and shape and efficiency of the microlens. Minimum illumination is defined as the illumination required for minimum measurable pixel output at 30msec exposure with f2.0 lens aperature. Dynamic range is measured as the ratio of the maximum illumination that can be measured without saturating the pixel and minimum illumination with 30msec exposure. Sensitivity is measured as the resulting green pixel output under uniform white illumination at 4700 K. G_R G_B crosstalk is measured as the difference between green pixels from green-red and green-blue rows under uniform white illumination at 4700 K and is closely related to imager MTF. Pixel uniformity is measured as the standard deviation of pixel outputs when the average has a code count of 150 and under uniform white illumination at 4700 K and with proper gain adjustments on red, green and blue channels. Dark current was measured in the dark at room temperature with integration times ranging from 500msec to 2 sec.

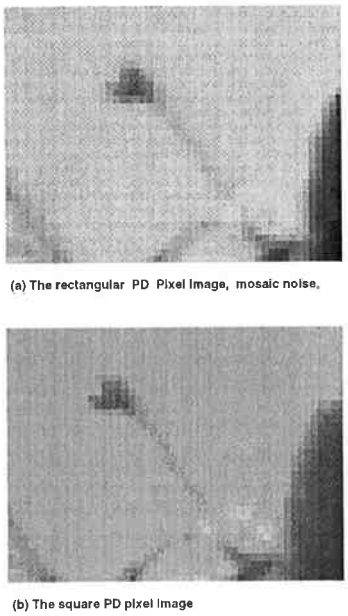
The optimized square PD pixel demonstrated significantly lower G_R G_B crosstalk as shown in Fig 5. These noise reductions also improve image compression efficiency and dynamic range. Although the square PD pixel had a slightly smaller PD, the higher efficiency microlens contributed to higher sensitivity compared to the rectangular PD pixel. Similarly, the square PD pixel showed better pixel matching as shown in Fig 6. DDS provides excellent cancellation of fixed pattern noise, and remaining pixel mismatches are primarily random.

The double slope ADC is currently still under testing. Preliminary results demonstrate that the ADC circuitry is fully functional and provides enhanced resolution and dynamic range.

6. CONCLUSIONS

A 640 × 480 VGA CMOS imager with a new optically improved pixel layout and 10b ADC bank using a double slope technique was designed and implemented in a modified 0.5 μm DRAM process. Photodiode shape and surface topology were considered in the pixel design and yielded significant improvement in the pixel optical performance.

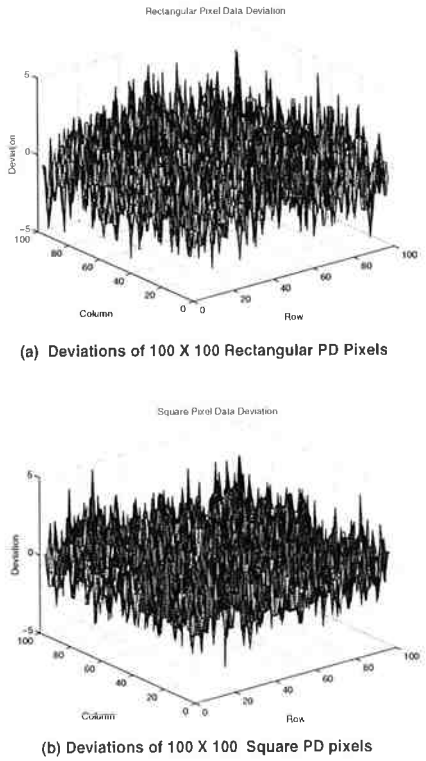
A die photograph of the implemented chip is shown in Fig. 7



(a) The rectangular PD Pixel Image, mosaic noise.

(b) The square PD pixel image

Fig. 5. Color mosaic noise due to the sensitivity difference between two green types.



(a) Deviations of 100 X 100 Rectangular PD Pixels

(b) Deviations of 100 X 100 Square PD pixels

Fig. 6. Deviations of pixels in a same frame.

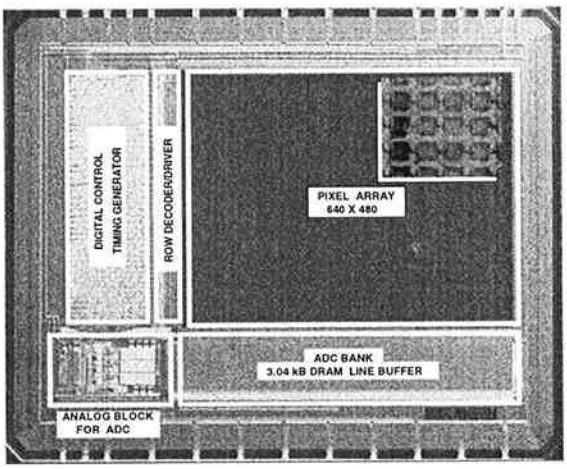


Fig. 7. Die photo of 640x480 CMOS imager.

7. ACKNOWLEDGEMENTS

The authors wish to thank Seong-Cheol Byun, Young-Min Lee and Seong-Bin Park in the Device Engineering Laboratory and Process Technology Laboratory of Hyundai Electronics for their support of this project. In addition, we wish to thank Duk-Won Lee for helping to prepare this paper and for his helpful comments.

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