

Analysis and enhancement of low-light-level performance of photodiode-type CMOS active pixel imagers operated with sub-threshold reset

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Noise in photodiode-type CMOS active pixel sensors (APS) is primarily due to the reset (kTC) noise at the sense node [1], since it is difficult to implement in-pixel correlated double sampling for a 2-D array. Figure 1 shows the pixel schematic of a photodiode APS. Signal integrated on the photodiode sense node (SENSE) is calculated by measuring difference between the voltage on the column bus (COL) - before and after the reset (RST) is pulsed. Lower than kTC noise can be achieved with photodiode-type pixels by employing "soft-reset" technique. Soft-reset refers to resetting with both drain and gate of the n-channel reset transistor kept at the same potential, causing the sense node to be reset using sub-threshold MOSFET current. However, lowering of noise is achieved only at the expense higher image lag and low-light-level non-linearity. In this paper, we present an analysis to explain the noise behavior, show evidence of degraded performance under low-light levels, and describe new pixels that eliminate non-linearity and lag without compromising noise.

Reset noise at the sense node can be estimated from the time-dependence of the probability distribution function (F_n), defined as the probability of finding n electrons on the sense node at a particular moment. In weak-inversion, the current is given by: $I = \exp\left[\frac{q \cdot \Delta V}{m k T}\right]$; where ΔV is the voltage difference between V_{GS} (or V_{SD}) and the threshold voltage (V_T), kT/q is the thermal potential (ϕ_T), and m is the non-ideality factor. Since $V_{DS} \gg \phi_T$, the reverse current is minimal, making the current flow essentially unidirectional. Then:

$$\frac{\partial F_n}{\partial t} = F_{n-1} g_{n-1} - F_n g_n \quad (1)$$

where g_n is the probability per unit time of adding an electron in presence of n electrons. The variance in the average number of electrons (\bar{n}) on the sense node can be computed from equation 1 to yield:

$$\frac{d\sigma^2}{d\bar{n}} = 1 + 2 \frac{dg}{dt} \frac{1}{g} \sigma^2 \quad (2)$$

For weak-inversion condition, $g_n \sim \exp[-\beta \cdot n]$, where $\beta = q^2/mkTC$. Equation 2 can then be solved to yield:

$$\sigma^2 = \frac{1}{2\beta} \left[1 - e^{-2\beta \Delta n} + 2\beta e^{-2\beta \Delta n} \sigma_0^2 \right] \quad (3)$$

where σ_0^2 is the variance at the onset of the reset process, and Δn is the average amount of electrons added to the sense node. For a photodiode type APS under soft-reset, $\sigma_0^2=0$ for a given frame, and

$$\sigma^2 = \begin{cases} \Delta n & ; \quad \text{for } \beta \cdot \Delta n \ll 1 \\ mkTC/2 & ; \quad \text{for } \beta \cdot \Delta n \gg 1 \end{cases} \quad (4)$$

In other words, if the amount of charges added is small, reset noise is determined by the shot-noise in the amount of electrons, and can be substantially smaller than kTC. On the other hand, if Δn is large, reset noise approaches $mkTC/2$. If $m=1$, there is a factor of 2 reduction in variance for soft-reset.

The reduction in reset noise is caused by the feedback inherent to the reset mechanism. For an exponential current flow over the barrier, instantaneous current flow is decreased sooner there is an increase in the node potential. As a result, the distribution of electrons narrows as the reset (under weak-inversion) progresses, causing sub-kTC reset noise. Another advantage of soft reset is high Power Supply Rejection Ratio (PSRR), since the reverse current is negligible, preventing power supply fluctuations to interact with the sense node.

Soft-reset affects imager behavior both under steady-state and dynamic conditions. Figure 2 shows a possible timing diagram (for still imaging mode) showing the reset (RST) pulse and the pulse (SHR) indicating when the reset level is sampled. Keeping the RST high during the idle phase (t_{idle}) enables flushing of unwanted charges, but steady-state linearity is greatly degraded. The response non-linearity is due the weak-inversion

current that causes SENSE to charge up in a slow logarithmic manner during the idle phase (t_{idle}). If the current during the integration phase (t_{int}) is small, SENSE is not discharged enough for the subsequent reset to affect the potential of the sense node. Consequently, the difference between the signal and the reset levels becomes extremely small for small signals, causing response non-linearity at low-light levels.

Figure 3 shows the response measured from a large format (512x512) imager operated with the timing shown in figure 2. The response "dead-zone" is clearly seen for low-light levels. The dead-zone can be virtually eliminated by holding the reset low during t_{idle} , which prevents biasing the reset transistor in deep sub-threshold condition. Even then, the response non-linearity at low-light levels can be significant. This can be judged from the SPICE simulation results as shown in figure 4. It plots the simulated potential variations on SENSE as it is periodically reset for different voltage excursions during the reset OFF state. The simulations indicate that the actual reset level is higher by more than 30 mV under low-light-levels, causing an order of magnitude increase in non-linearity at steady-state. Under dynamic lighting conditions, the reset level will vary from one frame to another depending upon the signal integrated in the previous frame. The variation of the reset levels between successive frames is the measure of image lag.

Figure 5(a) and 5(b) show the circuit schematics of the flushed and the hard-to-soft (HTS) photodiode APS pixels respectively. The flushed photodiode pixel consists of an additional line (\overline{HTS}) that controls the potential at the drain of the reset transistor. There are no changes to the pixel for the HTS photodiode APS. However, the power supply (Vdd) is routed to each column through a n- and p-channel transistor as shown in figure 5(b). Figure 6 shows the pixel timing diagram. HTS is a row-decoded signal for the flushed photodiode pixel, and it is a common signal for the HTS pixel. Momentarily pulsing HTS with the reset (RST) pulse ON causes the pixel to be reset first in hard-reset, followed by a soft-reset. For the HTS pixel, the hard-reset level is determined by the sizing of the transistors, and is set to approximately $1/2 \cdot V_{dd}$.

The hard reset erases the pixel memory, as a result of which the soft-reset level reaches the same level irrespective of the photosignal strength, as shown in PSPICE simulations in figure 7. Unlike in figure 4, the soft-reset level no longer depends upon voltage excursions at SENSE. HTS mode of operation does not affect the reset noise, since equation 3 indicates that as long as Δn is large, the contribution from the initial variance (due to hard-reset in this case) is minimal. In other words, to a first order, the imager performance does not depend upon the actual value of the hard-reset level.

In order to experimentally prove out the concept, a 128x128 test imager with 12 μm pixels was designed, and fabricated in 0.5 μm CMOS technology. The imager contains different pixels to allow investigation of four different modes of operation: soft-reset, hard-reset, HTS and flushed. Figure 8 shows the measured response linearity, the imager being operated in double-delta sampling mode [1]. The test results demonstrate that the imager operated in soft-reset mode exhibits significant low-light level non-linearity, whereas it is undetectable in the other three modes down to the read noise levels ($\sim 250\text{-}400 \mu\text{V r.m.s.}$). Figure 9 shows that the image lag is high ($\sim 2\%$) for large signals (in the previous frame), sharply dropping to less than 1% for smaller signals. It is, however, undetectable for the other three operating modes. Figure 10 shows the measured noise for hard-reset and HTS mode of operation. The noise performance closely follows the model, with the noise for hard-reset mode being given by \sqrt{kTC} , and less than $\sqrt{0.5kTC}$ for HTS mode.

In conclusion, we have demonstrated two photodiode pixel approaches that provide low reset noise and high PSRR, without sacrificing response linearity or introducing image lag. The measured noise data shows excellent agreement with the noise model developed.

ACKNOWLEDGMENTS:

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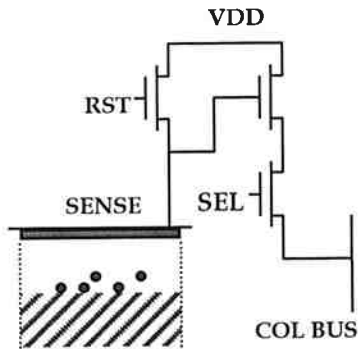


Figure 1. Schematic of a photodiode-type CMOS APS pixel.

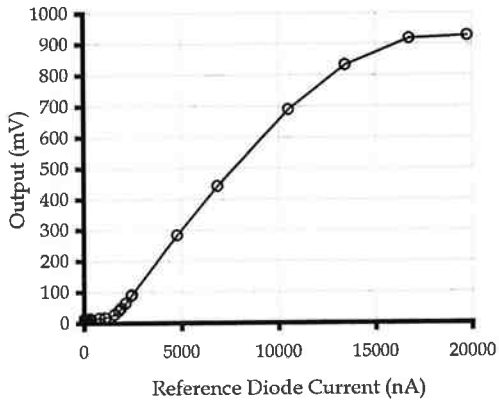


Figure 3. Response non-linearity with the pixel held in reset state during idling phase.

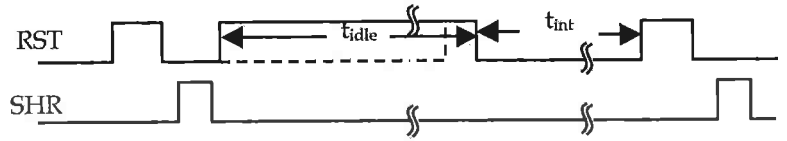


Figure 2. Timing diagram for imager running in digital still mode.

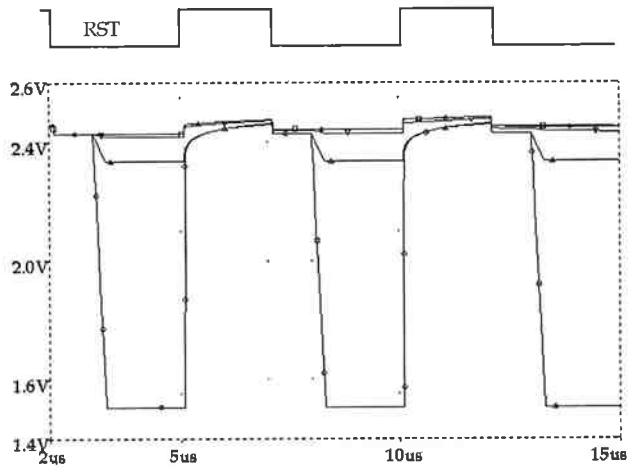


Figure 4. SPICE simulation showing the sense node potentials for different sense node signal excursions as the pixel is periodically reset.

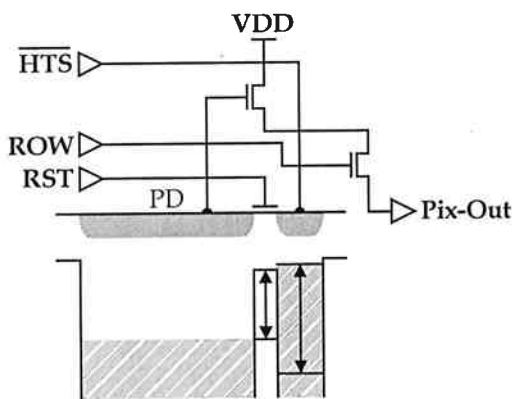
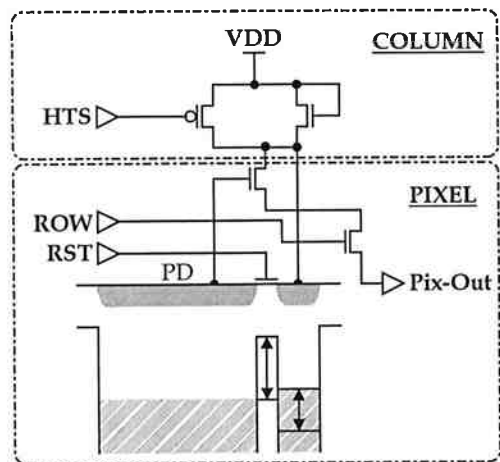


Figure 5. (a) Schematic of the flushed photodiode APS pixel;



(b) Schematic of the HTS photodiode APS pixel.

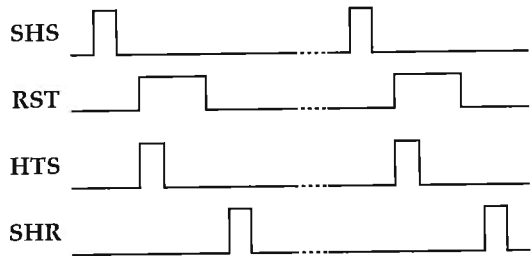


Figure 6. Pixel timing diagram.

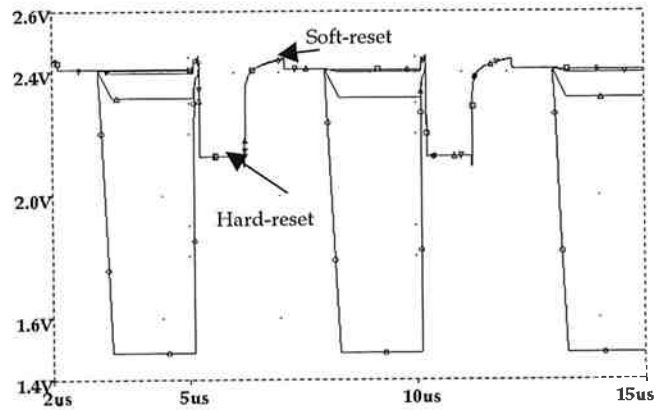


Figure 7. SPICE simulation showing the sense node potentials for different sense node signal excursions as the pixel is periodically reset.

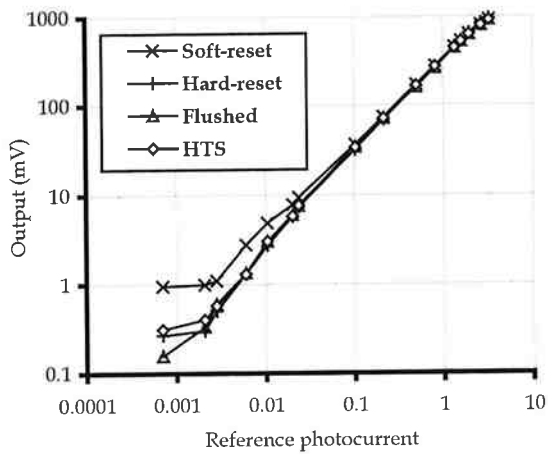


Figure 8. Measured Photodiode APS pixel linearity.

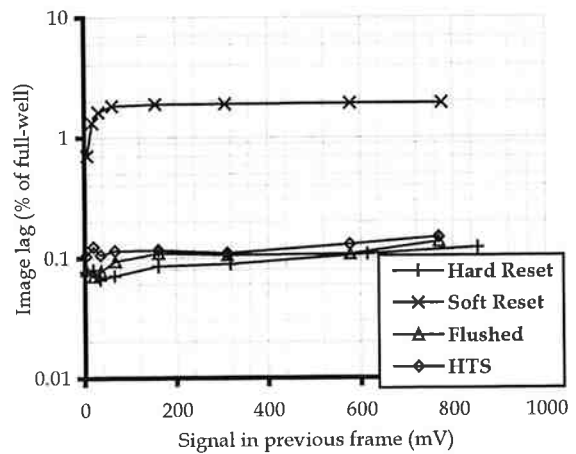


Figure 9. Measured image lag from different photodiodes.

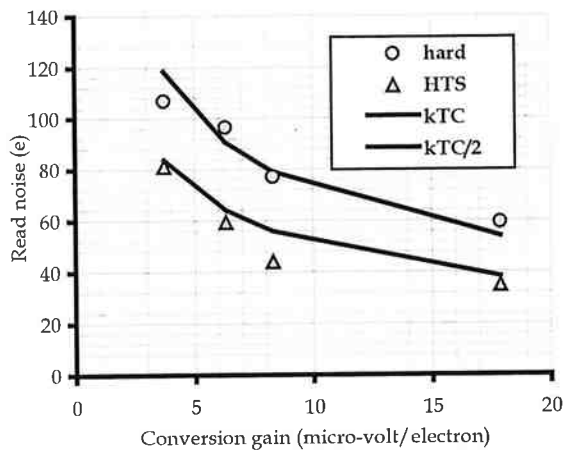


Figure 10. Noise as a function of the pixel conversion gain.