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Technology and Performance of VGA-Format Progressive IT-CCD imagers with Double Transfer Gate Four-Phase Pixel Structure

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Abstract

A new pixel structure has been developed to reduce the readout voltage in the 4-phase progressive scan IT-CCD image sensors. A triple poly-silicon technology is used to fabricate 4-phase VCCD gate structure. During the readout operation, conventional 4-phase structure requires higher readout bias to eliminate the image lag resulting from the narrow gate width compared to 3-phase structure. To have larger effective gate width, double transfer gate(DTG) structure was employed. But this method requires gate shielding in the photodiode-photodiode(PD-PD) interface region to avoid the potential barrier reduction due to the readout pulse. A 1/3-inch 330k-pixel CCD imager was fabricated, and its experimental results are presented with the 3-D simulation results.

1. Introduction

Recently square-pixel progressive scan(PS) CCD image sensors have attracted special interests because of the rapid growth of a digital camera market. Compared to the interlace scan(IS) type CCDs, PS CCD image sensors suffer mainly two problems. Firstly, performance degradation occurs due to reduced charge handling capacity in the vertical CCD(VCCD) channel. Secondly, fabrication of shrinked VCCD gates became more difficult. It has been reported[1] that 4-phase PS CCD structure is advantageous over the 3-phase PS CCDs in terms of the charge handling capacity. However, it is noted that 4-phase CCD structure has a narrower transfer gate(TG) and needs higher TG bias to eliminate the potential barrier at the PD-VCCD interface. Otherwise, charges can not transfer 100% from PD to VCCD channel, resulting in a large image lag.

To solve this problem, we have developed a modified pixel structure which can eliminate the above bottleneck effect by increasing the effective TG width by a factor of two. Employing this new structure, the potential barrier at the PD-VCCD interface can be eliminated and charge transfer from PD to VCCD is enhanced even with the lower readout bias.

2. Device Structure

As shown in the Fig.1, our 1/3-inch progressive scan 661(H) x 495(V) IT-CCD imager has 4-phase pixels measuring 7.4um x 7.4um. This device has been fabricated using n-epi wafer as a substrate so as to have a vertical overflow drain(VOFD) structure as shown in Fig.2. On-chip color filter consists of RGB dye filter layers and micro-lens layer is placed on the top of the device for the sensitivity enhancement. We

adopted a 3-polysilicon 4-phase gate electrodes for the VCCD. Fig.3 and Fig.4 show the cross sectional view of both PD-PD interface and VCCD region. Difficulties of forming a 3-poly-silicon structure are summarized as the following.

Firstly, TG should be shielded from the substrate by another poly-silicon layer as it passes by the PD-PD interface to avoid the influence on the potential barrier profile due to the TG plus. Secondly, PD-PD interface region should be minimized to have an enough optical fill factor.

The first consideration above is not necessary for the single transfer gate(STG) structure, because readout gate is the third poly-silicon layer and it is already paced on the first or second poly-silicon layer. But, in the conventional structure shown as Fig.3(a), second poly-silicon electrodes are not shielded from the silicon and can not be applied a readout pulse. Therefore, we have developed a modified structure as shown in Fig.3(b) and Fig.4 such that one of the second poly-silicon electrode is shielded by the first poly-silicon electrode while the other is placed on the gate oxide with a slight overlap with the first poly-silicon electrode.

For the second consideration, we have compared the PD-PD space from the process point of view, it turns out that we can not see any significant difference between the DTG structure and the conventional STG structure.

3. Device Simulation

Fig.1 represents a 1/3-inch 4-phase DTG 330k-pixel IT-CCD pixel structure we have used as a simulation model. Device simulation was performed using SPECTRA[2] with a doping profile provided by Suprem3 simulation. To observe the different results between STG and DTG structure, bias is applied to each of the electrodes as shown in Tab.1. Maximum potential profiles of two different pixel structures are shown in Fig.5 and Fig.6. It is noted that in Fig.6 potential barrier at the PD-VCCD interface is eliminated at the same TG bias when DTG method is employed. If we vary the TG bias to determine the minimum point of no barrier condition, it turned out that 12v and 9v are obtained for STG and DTG case, respectively.

4. Experimental Results

The device characteristics are summarized in Tab.2. When we measure the signal output as we vary the readout bias, we obtained different results between STG and DTG method as we expected from the simulations. Signal output saturates at 10v and 13v for DTG and STG method, respectively. This value is a good agreement with the simulation results.

5. Conclusion

We have developed a VGA-format progressive scan IT-CCD image sensor with a 4-phase DTG pixel structure. The pixel structure was designed based on the 3-D device simulation using SPECTRA. The device was fabricated by employing 3-polysilicon process, and from the measurements we confirmed that readout voltage could be reduced by DTG method without sacrificing the image lag characteristics.

References

(1) T. Yamaguchi et al., "1/3-inch 330k Square-Pixel Progressive Scan IT-CCD", IEEE CCD Workshop on Charge Coupled Devices and Advanced Image Sensors, April 1995.

(2) H. Mutoh et al. "A 2/3 inch 800k Pixel Color Image Sensor", ITEJ Technical Report, vol. 13, No. 11, pp. 73-78, TEBS '89-13, ED '89-17, Feb. 1989.

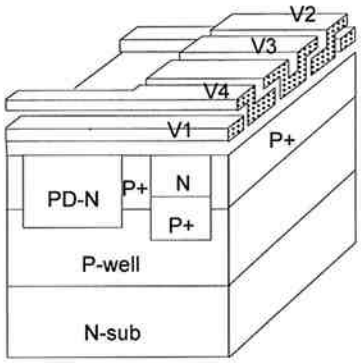


Fig. 1 1/3-inch 330k-pixel PS-CCD cell structure

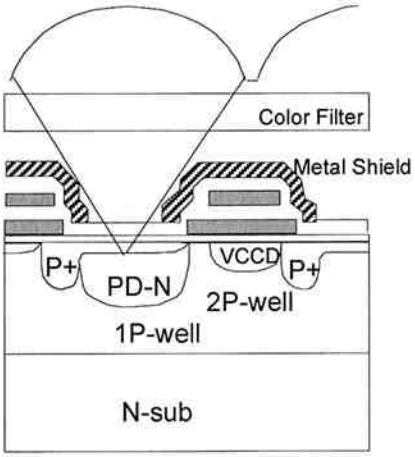


Fig. 2 Horizontal cross-sectional view of the pixel structure

(a)STG structure (b)DTG structure

Fig. 3 Cross sectional view of poly-silicon structure at the PD-PD interface. Shaded electrodes denote the TG's.

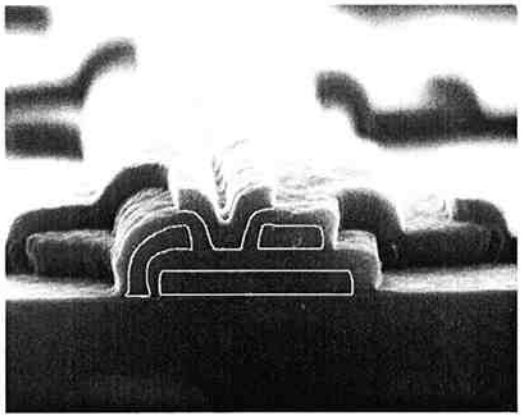


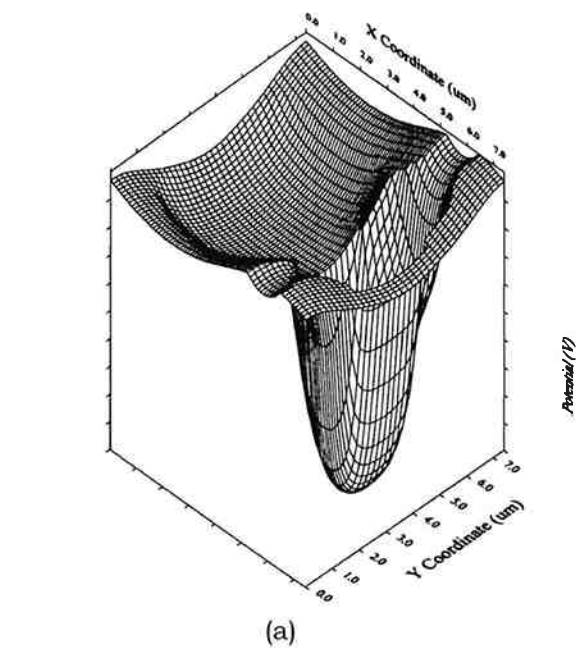
Fig. 4 Vertical cross-sectional view of the pixel structure

	V-sub	V1	V2	V3	V4
STG	10V	-9V	0V	9V	-9V
DTG	10V	-9V	9V	9V	-9V

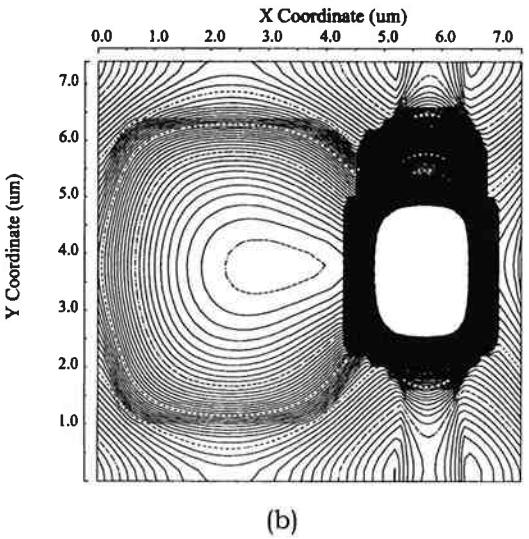
Table 1 Bias condition in the simulation model.

Optical format	1/3 inch
Effective pixels	661x495
Pixel size	7.4umx7.4um
Horizontal resolution	480 TV line
Vertical resolution	480 TV line
Sensitivity	950mV/lx
Saturation voltage	730mV
Dark signal voltage	< 0.5mV(60°C)
Smear	-85dB

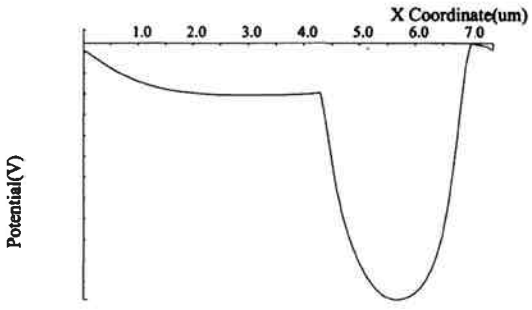
Table 2 Device Characteristics



(a)

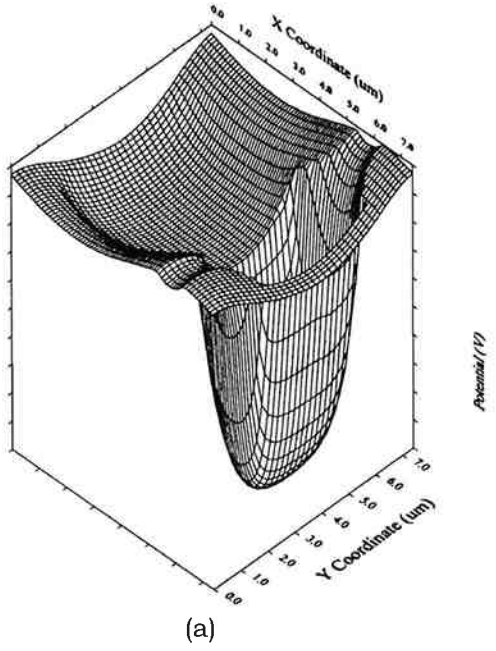


(b)

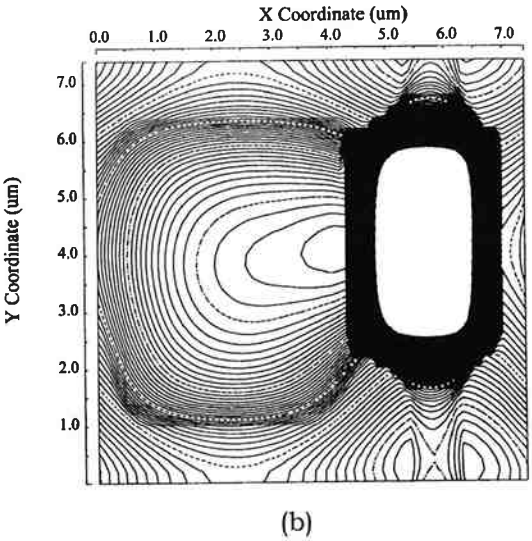


(c)

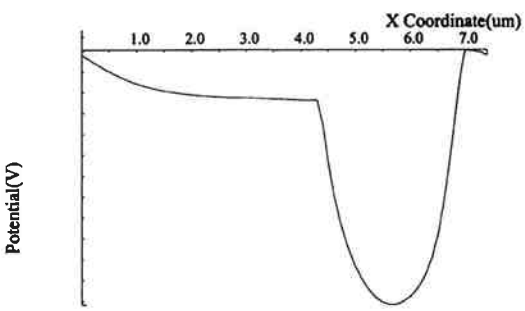
Fig. 5 Simulated maximum potential profiles of STG structure.



(a)



(b)



(c)

Fig. 6 Simulated maximum potential profiles of DTG structure.