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Correlation Between Leakage Current and Overlap Capacitance in a-Si:H TFTs

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Abstract

The reverse leakage current and parasitic capacitances in amorphous silicon thin-film transistors (a-Si:H TFTs) lead to adverse effects on imaging array performance. The capacitances, Cgs and Cgd, consist of geometric and bias-dependent components, arising from overlapping of gate and source/drain electrodes (Fig. 1) and charge transport by virtue of a large electric field across a highly reverse biased p-i-n diode at the drain region (Fig. 2). It is this reverse biased p-i-n diode that is the main constituent for leakage and which influences Cgs and Cgd in the TFT. In this paper, we show, through systematic experimental studies, that the capacitances and leakage current vary consistently with overlap length, effective channel length, and a-Si:H layer thickness.

Introduction

When used as an addressing switch in pixelated arrays, it is essential for the TFT to prevent current flow in its off state (Vg < 0). But a small leakage current (Fig. 4) flows to undermine charge retention on the sensor. In addition, the capacitances Cgs and Cgd (Fig. 3), allow the gate voltage to feed through to the output as well as consume signal charge from the sensor to degrade pixel sensitivity. In order to grasp the correlation between these parasitic effects, the off-state characteristics of the TFT must be clearly understood from a charge perspective. Previously we reported [1,2] the formation of a parasitic reverse-biased p-i-n diode at the drain region. The large electric field across its intrinsic region, stemming from large gate-drain biases, leads to significant charge generation and conduction. This region has been identified to be the key factor that influences both the leakage and parasitic capacitances. Measurement data reveal that the leakage current and capacitances are correlated; they vary consistently with overlap length, gate and drain biases, effective channel length, and a-Si:H layer thickness.

Qualitative Charge Transport Picture

For negative gate and positive drain voltages, Vdg > 0, holes accumulate at the a-Si:H/gate nitride interface, and consequently, electrons at the a-Si:H/top nitride interface (Fig. 2). This results in formation of a distributed p-i-n diode along the channel from the source to the drain. However, only the parasitic p-i-n diode near the drain region has a significant effect on both leakage current and capacitance, due to the relatively large voltage drop across the gate and drain. For relatively small biases, Cgs and Cgd should be just equal to their respective overlap values, Cgso and Cgdo (Figs. 1 and 3). But for large Vdg (as seen later in Fig. 5), one observes an increase in capacitance from the geometric value; this increase associated with charge accumulation [3,4]. In our case, the accumulation stems from charge generation and transport induced by the gate-drain electric field.

Measurement Results and Discussion

At low and intermediate gate and drain voltages, the leakage current increases slowly (Fig. 6) and has almost no effect on the capacitance at the source side. At higher gate and drain voltages, the high electric field

between drain and gate electrodes leads to generation of electrons and holes, which are subsequently swept across the diode to increase the leakage current. This leaves the holes to conduct through the channel, at the a-Si:H/gate nitride interface, to the source side where they recombine to produce a drain-source current. Consequently, due to the augmented hole concentration at the source end, capacitance at the source side increases (see Fig. 5). The capacitance also increases with increasing Vds. Here, the lateral electric field between drain and source increases, causing hole conduction to increase resulting in increased hole concentration at the source side.

Figures 7 and 8 show that Cgs and leakage current increase with increasing overlap length. In the region, Vgs $\leq$ 0V, the capacitance is solely dependent on the geometric overlap. As the overlap increases, capacitance increases. The rise in leakage can be attributed to the increase in the effective area of the high field region, which allows for increased charge generation and conduction to enhance the leakage current.

From previous work [1], we found that for TFTs with a very thin (~25nm) a-Si:H layer, the leakage current increases rapidly with gate voltage. Here, the barrier width of the p-i-n diode is small and trap-assisted tunneling dominates to cause diode conduction to increase rapidly. This in turn increases the hole concentration at the source side by conduction through the channel. From the corresponding capacitance behavior shown in Fig. 9, we observe that there is rapid increase in capacitance particularly at high drain voltages. Here, in correspondence to the leakage current (see Fig. 10), the high hole conduction through the diode increases the concentration of holes at the source end leading to a strong dependence of Cgs on Vgs and Vds.

When the effective channel length of the TFT is reduced from 25 μm to 9 μm (see Figs. 11 and 12), the lateral electric field between the drain and source increases. This effectively allows more holes to flow across the channel at lower gate and drain voltages, increasing the concentration of holes at the source. Consequently, the capacitance at the source side increases at lower gate voltages. Also, the flat portion of the capacitance characteristic increases for increasing Vds and this confirms that the lateral electric field enhances hole transport.

Conclusions

The key to the correlation between leakage and capacitance is the parasitic p-i-n diode formed near the drain region. At large drain-gate voltages, there is significant charge generation in its intrinsic region, which we believe is due to Poole-Frenkel emission, as gathered from the observed dependence of the leakage current on electric field (stemming from Vdg). Here, the generation rate within the depleted intrinsic region is not constant but enhanced by the electric field.

Acknowledgements

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References

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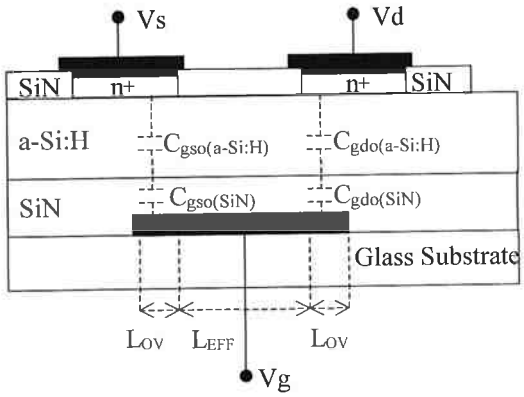

Figure 1: Schematic of a-Si:H TFT showing the geometric capacitances at the drain and source.

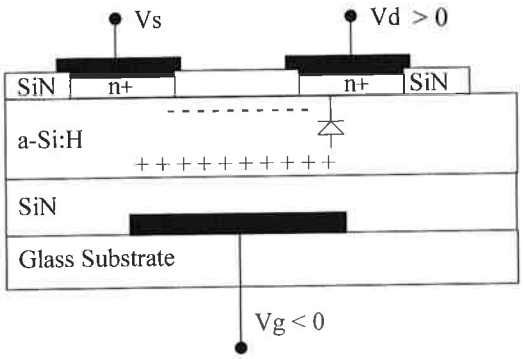

Figure 2: Charge picture of a-Si:H TFT in its off-state indicating formation of a p-i-n diode at the drain region.

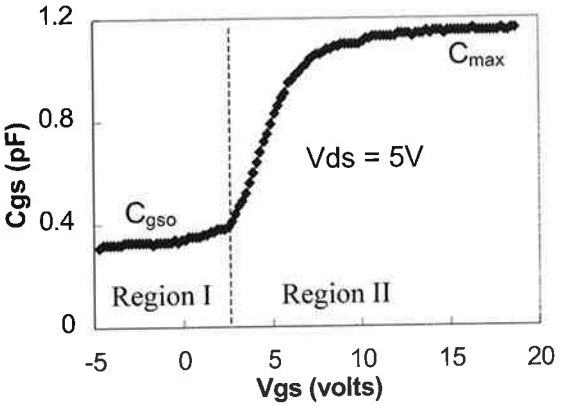

Figure 3: Typical capacitance-voltage characteristic of TFT with an overlap of 2μm.

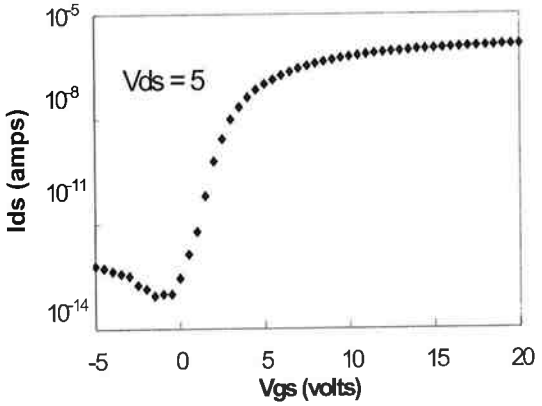

Figure 4: Typical transfer characteristic of TFT with an overlap of 2μm.

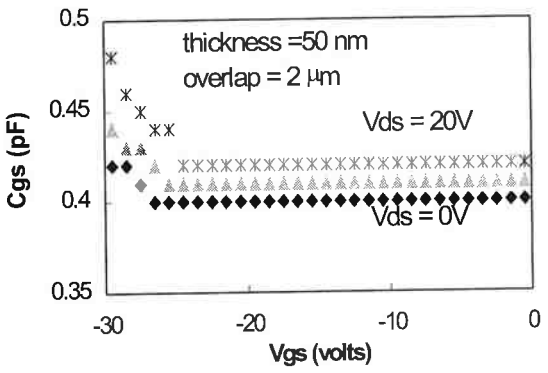

Figure 5: Gate-to-source capacitance vs gate voltage for different drain voltages (Vds = 0, 10, 20 V) indicating an increase in capacitance for increasing gate and drain biases.

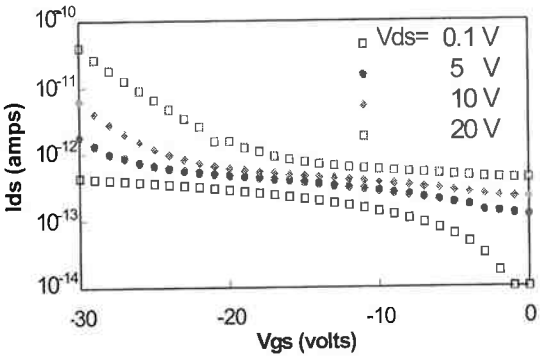

Figure 6: Drain current vs gate voltage for different drain voltages indicating an increase in leakage current for increasing gate and drain biases.

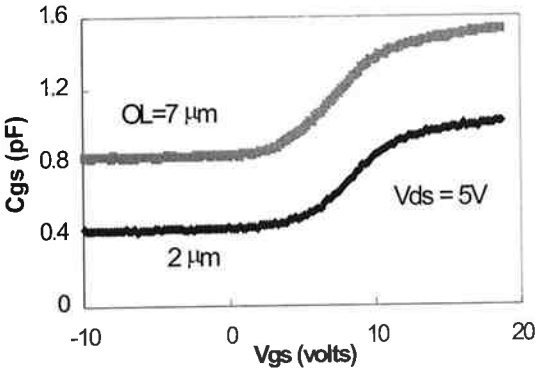

Figure 7: Gato-to-source capacitance vs gate voltage for TFTs with different overlap length.

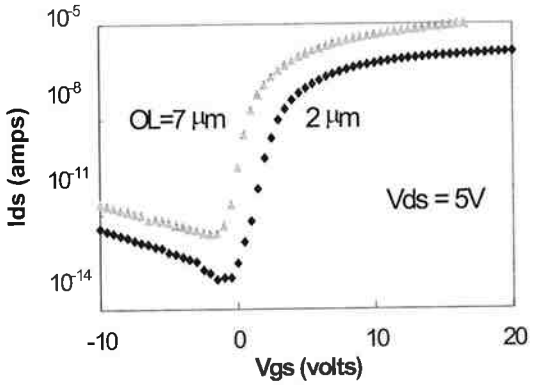

Figure 8: Drain current vs gate voltage for TFTs with different overlap length.

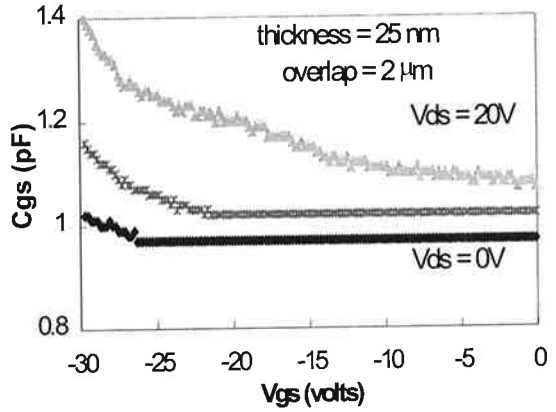

Figure 9: Gate-to-source capacitance vs gate voltage for different drain voltages (Vds = 0, 10, 20 V) for a TFT with a-Si:H layer thickness of 25nm.

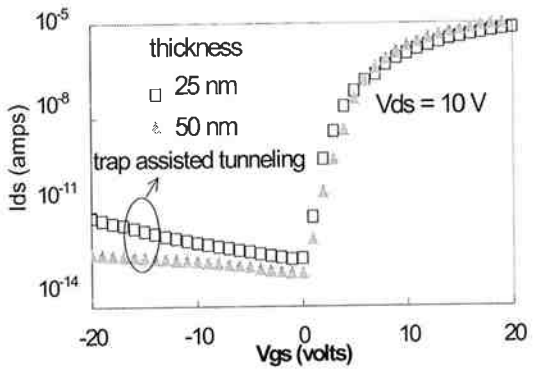

Figure 10: Drain current vs gate voltage for different a-Si:H layer thickness indicating the dominance of trap-assisted tunneling.

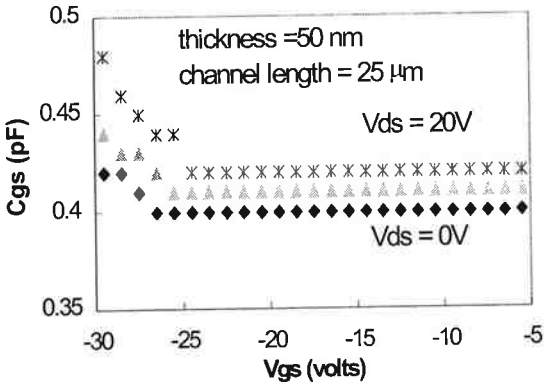

Figure 11: Gate-to-source vs gate voltage for different drain voltages (Vds = 0, 10, 20 V) for a TFT with channel length of 25μm.

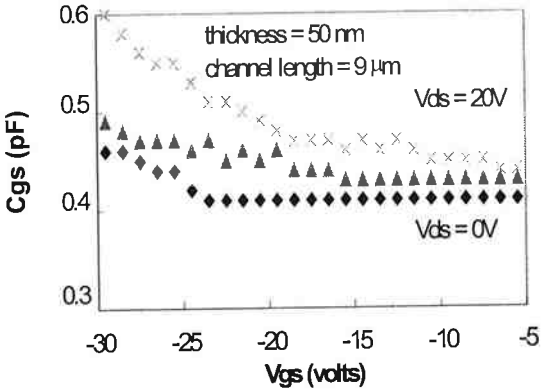

Figure 12: Gate-to-source capacitance vs gate voltage for different drain voltages (Vds = 0, 10, 20 V) for a TFT with channel length of 9μm.