P12 A Passive Photodiode Pixel with Memory

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I. INTRODUCTION

Passive photodiode sensors are characterized by low fix-pattern noise (FPN), high fill factor and excellent blue response. However, compared to other pixel structures, such as the photogate active pixel sensors (APS), they lack the ability to store the sampled[1] charge value within the pixel separate from the photosensitive device. This ability is required in some cases, e.g. to implement an electronic shutter which acts simultaneously over a whole array of pixels ("snap-shot" mode). Contrary to the normally implemented progressive scan mode of operation, an electronic shutter effectively avoids image smear whenever there is a relative motion in the scene. This ability is for instance required in high speed tracking applications.

Previous efforts implementing in-pixel memory have mainly focused on active pixel sensors. [1] describes a photodiode APS structure with the in-pixel memory implemented using a MOS-capacitance. In the pixel, the photodiode and the memory is separated by a NMOS pass transistor. However, a snap-shot mode of operation is not implemented, instead each row of in-pixel memory is updated in a progressive scan mode. The use of an APS enables non-destructive reading of the memory capacitor. [2] describes a passive photodiode structure with in-pixel memory used for motion detection. This design also does not implement a true snap-shot mode of operation, instead a progressive scan mode is used. In this case the use of passive pixels prevent non-destructive reading of the memory. True snap-shot sensors has been reported in for instance [3] and [4]. [3] uses a photodiode APS similar to the one described in [1], though in this design a snap-shot mode of operation is implemented by simultaneously resetting the photodiodes and, after the integration period, simultaneously pulsing the NMOS memory access transistor. In [4] a snap-shot photogate APS is described. By clocking a traditional photogate APS in a special way a snap-shot mode of operation is achieved. Other efforts using non-standard CMOS processes has also successfully implemented in-pixel memory. For instance, in [5] a CMOS/EEPROM process is used to integrate an analog nonvolatile memory to be used for FPN suppression in each pixel.

In this paper we present experimental results on a passive photodiode pixel which includes a separate in-pixel capacitor that acts as a memory. The pixel can be operated in a snap-shot mode, however multiple readings of the memory is prevented by the passive nature of the pixel.

II. PIXEL DESIGN

The principal pixel circuit is shown in Figure 1.

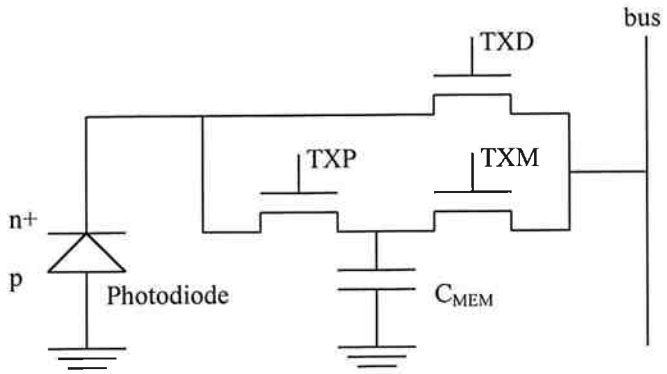

Figure 1. *Pixel with memory capacitor.*

[1] Now with Photobit Corporation, Pasadena, CA

A number of 128*16 pixels are connected to a set of column charge integrating amplifiers. The test chip further includes internal logic to enable pixel addressing and an 8-bit single slope AD-converter in each column.

Before exposure, the photodiode and the memory capacitor is reset (precharged) by momentarily closing all the switches while the column bus is driven to a nominal voltage by the charge integrating amplifiers. The switches are then released. By resetting all pixels simultaneously the integration of all pixels are started at the same time. After the selected exposure time during which the diode will be partially discharged, one of two possible actions take place. Either the sensor is operated in normal progressive scan mode in which the photodiode rows are sequentially read out by activating the TXD-switch. The TXD-switch is common for all pixels in a row. This is the traditional way to operate the passive pixel sensor [6]. To enable a snap-shot mode of operation all the TXP-switches are pulsed which results in a charge sharing between the photodiode capacitance and the memory capacitance, C_{MEM}. The charge stored on the memory capacitance now reflects the amount of light that has hit the diode during the exposure time. Thus the sensors memory capacitances now contains a snap-shot image of the scene. To read out the snap-shot image the memory capacitors are scanned line by line by opening the TXM-switch for all pixels in a row. During this period the photodiodes continues to discharge.

The layout of the pixel is shown in Figure 2, note that only metal, poly and diffusions are plotted. The layout is implemented in a double metal double poly 0.6µm standard CMOS process. The terminals are indicated in the figure. *TXP*, *TXM*, *TXD* and *bus* corresponds to the terminals in Figure 1. The *GND* terminal grounds the bottom plate of the in-pixel POLY-POLY memory capacitor as well as the substrate. The *ABL* terminal provides an antibloom voltage for the antibloom transistor at the top of Figure 2. The large quadratic area in the middle is the photodiode which is implemented as an n+-diffusion in the p-substrate. The photodiode capacitance is calculated to 32fF. The rectangular shaped area to the right of the photodiode is the memory capacitor which is designed to match the 32fF of the photodiode. The pixel was designed to fit a quadratic pitch of 20µm. Compared to a conventional photodiode-only solution with the same optical and electrical parameters the pitch is about 65% wider. The drawn fill factor in the memory pixel is 25%. As much area as possible has been covered by metal, except over the photodiode, to act as a light-shield.

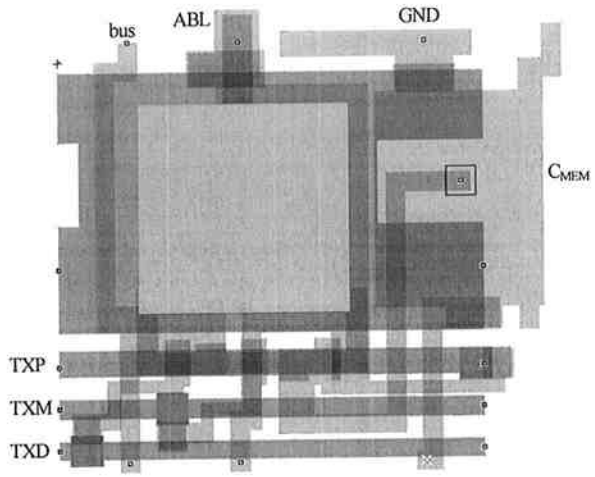

Figure 2. Photodiode layout.

III. RESULTS

By reading out the photodiode charge directly and alternatively through intermediate storage in the memory capacitor it was verified that the charge memory worked as expected. The amplitudes scaled accordingly with about a doubling of the levels when the storage was not involved. Snap-shot mode of operation was further verified. Figure 3. shows the gray level vs. exposure time when reading the pixel information from the in-pixel memory.

It should be noted that while the charge in the in-pixel memory capacitor is linearly proportional to the applied voltage the charge in the photodiode is not. The effective signal charge held in the photodiode, Q_{PD}, is dependent on the photodiode voltage as the following equation shows:

$$Q_{PD} = \int_0^{V_{PD}} c(v) \cdot dv \qquad c(v) = \frac{W \cdot L \cdot CA}{(1+\frac{v}{PB})^{MA}} + \frac{2 \cdot (W+L) \cdot CS}{(1+\frac{v}{PB})^{MS}}$$

Where, Q_{PD}=photodiode charge, V_{PD}=photodiode reverse bias voltage, c(v)=small signal capacitance given in the CMOS process parameters, W and L are the width and length of the photodiode, CA, CS, MA, MS and PB are process dependent parameters.

Due to the different charge-to-voltage characteristics of the memory capacitor and the photodiode a small non-linearity will result. For instance, when the TXP switch closes the voltage of the memory capacitor and the photodiode is equalized to V_{EQ}. Now, when reading the memory capacitor the sense amplifiers senses a charge given by $C_{MEM}*V_{EQ}$, but when reading the photodiode a charge given by Q_{PD} (EQ above, $V_{PD}=V_{EQ}$) is sensed.

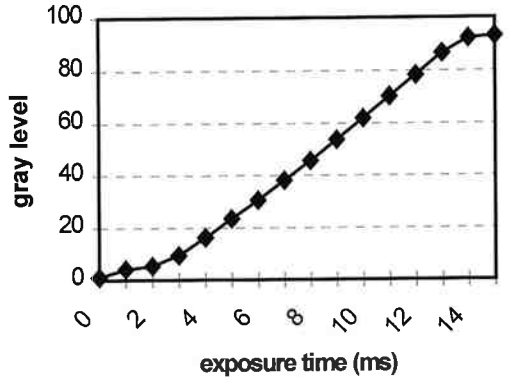

Figure 3. Gray levels vs. exposure time when reading the in-pixel memory.

Of special interest is to investigate the data retention integrity with respect to the illumination. Although the drain/source diffusions of the access transistors TXM and TXP are covered with metal, light-induced carriers in the substrate will diffuse to the diffusions and eventually discharge the capacitance. Note that this effect is dependent on the illumination of the scene and therefore the leakage is different at different locations of the sensor. Due to the relative long diffusion lengths the metal coverage is not sufficient and cannot be sufficiently increased to eliminate this leakage. One way to improve on the data retention would be to use a PMOS switch. Since the PMOS transistor lies in an n-well no stray carriers present under the well will reach the transistor. Unfortunately the use of a PMOS switch drastically reduces the fill factor. One could also design the photodiode as a p+-diffusion in an n-well and use PMOS switches. However it is known that these type of diodes suffer from lower sensitivity. Another way would be to cool the chip which will reduce the diffusion lengths. The leakage in this design was measured to 0.07 V/Lux*s at room temperature and it was verified that it was proportional to the illumination. In Figure 4 the leakage behavior of the memory pixel vs. exposure time under constant illumination is shown.

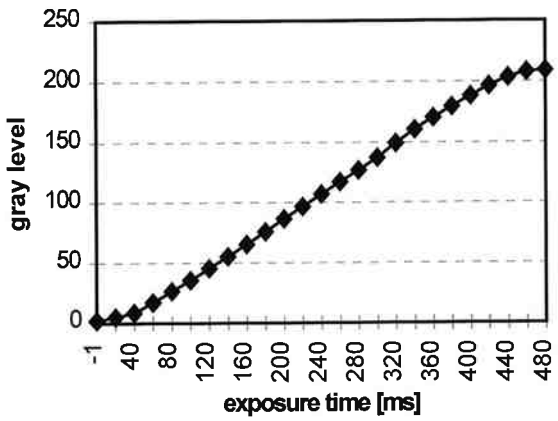

Figure 4. Leakage behavior vs. exposure time.

IV. APPLICATIONS

The memory photodiode finds its most obvious application in very high speed tracking applications. Normally, in tracking applications the frame rate is increased by only processing a small region-of-interest (ROI) in the image. The position of the ROI in the image is updated and maintained over time using tracking algorithms based on e.g. the Kalman filter. However, this approach requires that the frame rate is matched with the speed in such way that the object has not moved outside the ROI between each frame sample. If this situation occurs it is necessary to search the whole image to find the object again. Typically, the available processing time only allows for very simple image analysis operations to perform object detection.

In some high speed object tracking and analysis applications where it is necessary to first detect the object and then perform some more advanced image analysis it is not possible to maintain the very high frame rate and at the same time reach the goal of an extremely compact system. By using a frame memory (snap-shot mode) in the photodiode array itself it is possible to use a double scan procedure that first detects the object (ROI) and thereafter perform image analysis on the ROI only.

The first scan over the image array readouts the image to the memory cell at the same time performing very simple binary image operations for object detection. This results in a position for the object which provides the ROI for the second scan. In the second scan the memory is accessed and readout but only for the ROI defined by the first scan. During this second readout more advanced grey level operations are performed to classify the detected object. Using the double scan approach it is possible to track and analyze objects without restrictions to small ROIs and still maintain framerates of more than 500 frames per second in very compact system solutions.

V. CONCLUSIONS

A passive photodiode CMOS pixel was augmented to include a charge storage in the form of a separate capacitor. The extra space required increased the width of the pitch by about 65%. The new pixel could be read out either in conventional mode or in snap-shot mode. In the latter case the output levels will be about half of the dynamic range. Finally the data retention integrity under illumination was measured. Although a reasonable low value was measured, the leakage cannot be neglected in applications where long read-out times are used.

VI. ACKNOWLEDGEMENT

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VII. REFERENCES

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