P11: Design and Simulation of a CMOS Sensor Array

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Abstract

This work reports the design of an image sensor array with built-in data compression using the conditional replenishment video data compression (CRVDC) algorithm. The design was done based on a 0.8 CMOS process using a pixel-parallel architecture. As a test structure, we have simulated a 3 x 3 sensor array and examined its circuit performance.

Previously, a number of sensor or image compression circuits has been reported [1,2]. In this work, our design followed a similar approach. The individual pixel in the array is made up of a photodetector, a number of current mirrors, a fixed pattern noise reduction circuit, a memory, and 1 or 2 current comparators. The current mirrors were designed to have 10 bit accuracy, while the other circuits can handle no less than 8-bit accuracy. Two different pixel designs have been examined and Fig.1 shows one of them using a single current comparator. Fig.2 shows the simulation output when the input signal is sinusoidal. Good signal linearity was observed and the output dynamic range exceeded 75 dB. The settling time for this circuit was within 0.1 μs (10 MHz).

In the design of the 3 x 3 pixel array, we have used a variable threshold approach (i.e., the number of output pixels is fixed). Fig.3 shows the block diagram of the array which consisted of the pixel sensors, a driving pulse generator, a fixed-ratio controller, a current reference, a smart scanner, and two address decoders. A number of changes has been made to improve the circuit functionality; such as the addition of a reset switch to the smart scanner and the use of CMOS switches instead of conventional switches (this has the effect of reducing some of the voltage drop). One important design feature with the implementation of the CRVDC algorithm is the control of the variable threshold current. Two different fixed-ratio controller circuits have been examined and Fig.4a shows one of them (without voltage-current converter). The transient response of this circuit is shown in Fig.4b. Fig.5 shows the simulated readout and address signals from the 3 x 3 sensor array when input photocurrents are set to: 2.25 nA, 2.00 nA, 1.75 nA, 1.50 nA, 1.25 nA, 1.00 nA, 0.75 nA, 0.5 nA and 0.25 nA, respectively. The output to input (pixel) ratio is 6:9. In the first frame, since all of the sensor memories were initially reset, the pixel readouts are signals with the six largest photocurrents. In the second frame, the circuit picked up the first three remaining photocurrents since they registered the largest changes and three of the other photocurrents (they have the same amount of change).

[1] K. Aizawa et al, "On sensor image compression", IEEE TCSVT, Vol.,7, No.3, pp.543-548, 1997.
[2] K. Aizawa et al, "Computation image sensor for on sensor compression," IEEE TED, Vol.44, No.10, 1724-1730, 1997.

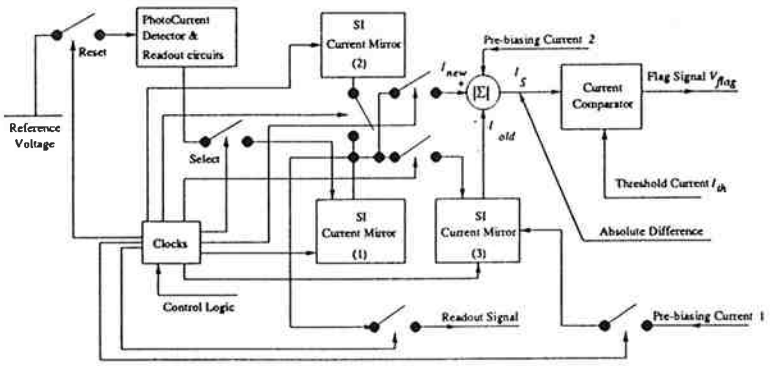


Figure 1 Block Diagram of the Single Pixel sensor (One current comparator approach)

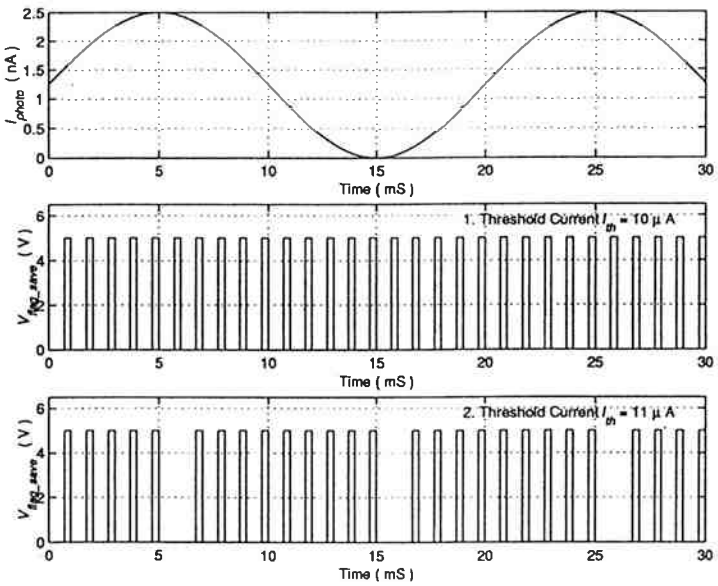


Figure 2 Transient Response of the Sinusoidal Photocurrent

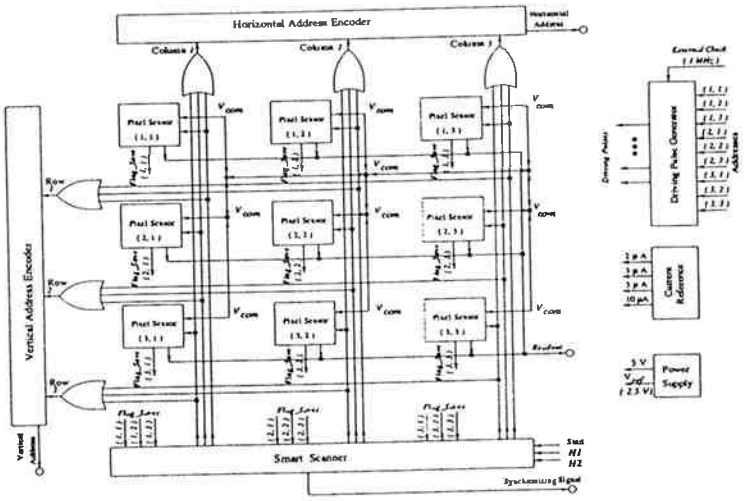


Figure 3 Block Diagram of the Sensor Array (Non-VC Converter Approach)

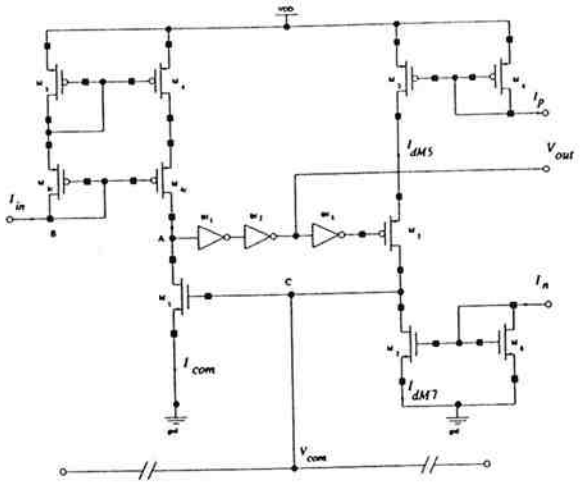
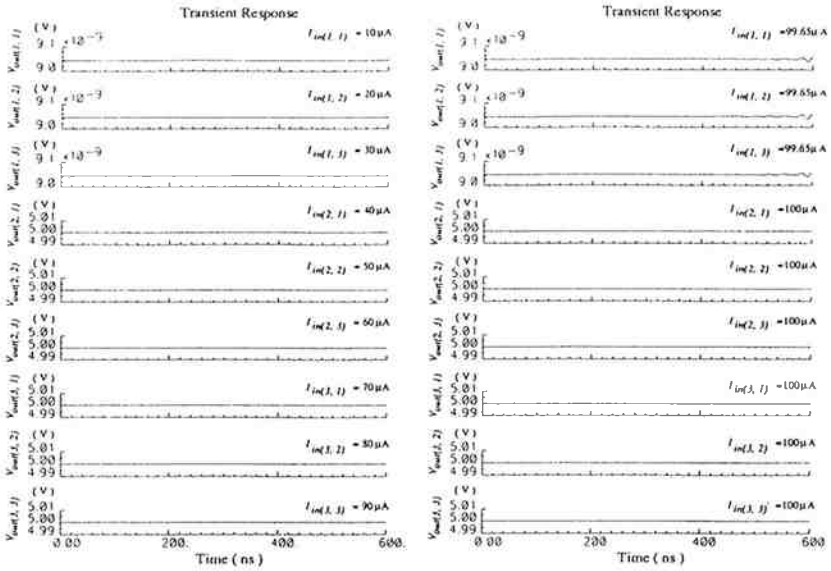
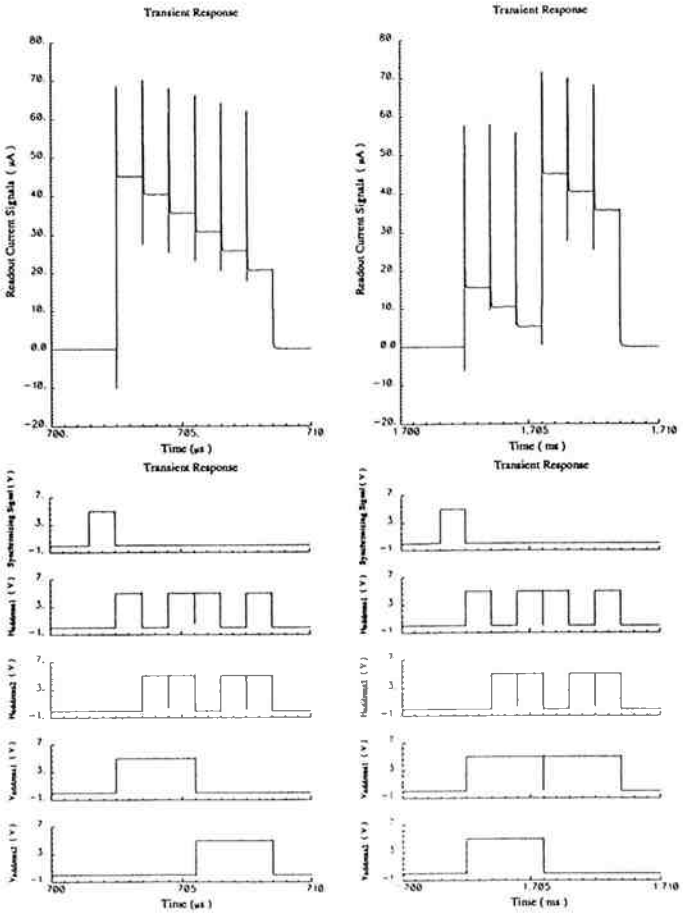


Figure 4 a One Element of the Fixed Ratio Controller (Non-VC Converter Approach)



(a) (b)

Figure 4 b Transient Response of the Fixed Ratio Controller (Non-VC Converter Approach)



(a) The First Frame (b) The Second Frame

Figure 5 The Readout Signals and Address Signals of the Sensor Array