

Takayuki Hamamoto †, Yoshikazu Ino † and Kiyoharu Aizawa ‡

†Science University of Tokyo  
 Dept. of Elec. Eng.  
 Shinjuku, Tokyo 162-8601, Japan  
 hamamoto@ee.kagu.sut.ac.jp

‡University of Tokyo  
 Dept. of Elec. Eng.  
 Bunkyo, Tokyo 113-8656, Japan  
 aizawa@hal.t.u-tokyo.ac.jp

1. INTRODUCTION

In this paper, we propose a novel smart sensor in which every pixel independently controls its integration time. The integration time is controlled so that it has higher temporal resolution and wider dynamic range.

A CCD sensor with electronic shutter[1] is capable of imaging at variable integration time. However, read out rate is fixed by timing of 30 frames/second and the integration time is constant for all pixels (Individual variation is not possible).

We have been investigating the adaptive-integration-time image sensor[2]. In the first 32×32 pixels prototype, the sensor has the circuits to detect motion and saturation, the integration time and output timing for each pixel are controlled by them. It can reduce image blur caused by moving objects in a scene as well as improving intrascene dynamic range.

In this paper, we describe a new adaptive-integration-time image sensor based on a column parallel architecture. It has 128×64 pixels. In this new prototype, the scheme to control integration time is much extended, and pixel pitch, processing speed and power consumption are much improved in comparison with our previous prototype. 7bits address encoder is newly implemented.

2. PRINCIPLE OF ADAPTIVE INTEGRATION TIME

Figure 1 shows the processing scheme in each pixel of the adaptive-integration-time image sensor. It has the circuits for detection of saturation and motion. Both integration time and output timing of the pixel value are controlled by any combination of three elements, which are motion detection, saturation detection and external signal. For example, integration time is controlled by motion or saturation, output timing is controlled by external signal. The integration time and

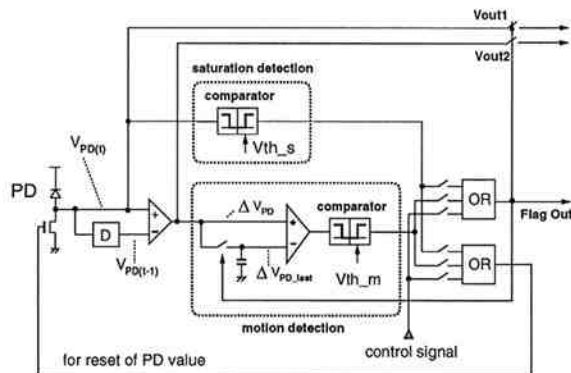


Figure 1: Description of processing in each pixel

output timing can be controlled pixel by pixel independently.

As shown in Figure 1, each pixel keeps integrating charge on photo diode (PD) until it activates PD reset signal. Detection of motion and saturation is processed every  $D$  seconds which is the minimum integration interval.  $D$  is set very small because the proposed sensor is intended to operate at high speed which is equivalent to more than 1000 fps for conventional image sensor.

The motion detection is done as follows. Firstly,  $\Delta V_{PD}$  which corresponds to the integration during the smallest interval  $D$  is calculated by the difference between  $V_{PD}(t)$  and  $V_{PD}(t - 1)$ .  $V_{PD}(t)$  corresponds to the integration on the PD from the last reset to the present.  $V_{PD}(t - 1)$  is the previous integration delayed by  $D$ .  $\Delta V_{PD}$ , in other words, can be considered as a pixel intensity at the rate of  $D$  integration time. A memory keeps  $\Delta V_{PD\_last}$  which is  $\Delta V_{PD}$  of the last output. If the magnitude of the difference between  $\Delta V_{PD}$  and  $\Delta V_{PD\_last}$  exceeds a threshold ( $V_{th_m}$ ), the pixel intensity significantly changes and the pixel is detected as moving.

The saturation is detected when  $V_{PD}(t)$  exceeds a threshold ( $V_{th_s}$ ). We can control  $V_{th_s}$  at every  $D$  timing so that this function is available as a simple A / D converter. The sensor also has the circuit to control both integration time and output timing of each pixel by external signals from outside of the chip.

By any combination of three functions, there are many imaging styles for our proposal. For example, if both integration time and output timing are controlled by only motion detection, the operation is equivalent to that of our image compression sensor[3][4][5]. If both are based on the combination of motion and saturation, it is equivalent to our first adaptive sensor[2]. In that case, the sensor controls the suitable integration time in each pixel, which results in no motion-blur and no saturation. It is expected to have high temporal resolution in the moving area, high SNR and wide dynamic range in the static area. On the other hand, variations of the integration time should be adjusted by post processing outside the sensor.

### 3. DESIGN OF COMPUTATIONAL ELEMENTS OF THE PROPOSED SENSOR

Figure 2 shows the block diagram of the adaptive integration time image sensor. This architecture separates transducer, memory and processing elements, and each column shares a processing element. Fill factor and power dissipation are almost comparable to an ordinary CMOS sensor. Using three vertical shift registers, the pixels and the memories are scanned line by line.

The proposed sensor has two horizontal shift registers. The upper shift register is used for outputting pixel data, which has two functions of a normal scanning and a smart scanning. One of the two is selected by a mode selection signal. Figure 3 shows the circuit of the shift register. When the normal scanning is chosen, upper paths of all pixels are selected to output the pixel intensities. When the smart scanning is chosen, if the flag signal is off, the bottom path is selected to skip the pixel without reading. It reads out the only activated pixels as a compact sequence.

In the case of the smart scanning mode, we use one of the two address information for image reconstruction. One is flag signals output by the bottom horizontal shift register in Fig.2, which operates at the rate higher than output rate of pixel intensities. The other is 7bits addresses output by an address encoder. The bottom shift register is also available for input of the external signals which control the integration time and output timing of each pixel from outside of the sensor.

Figure 4 shows the circuit designed for each pixel of the proposed sensor based on the column-parallel

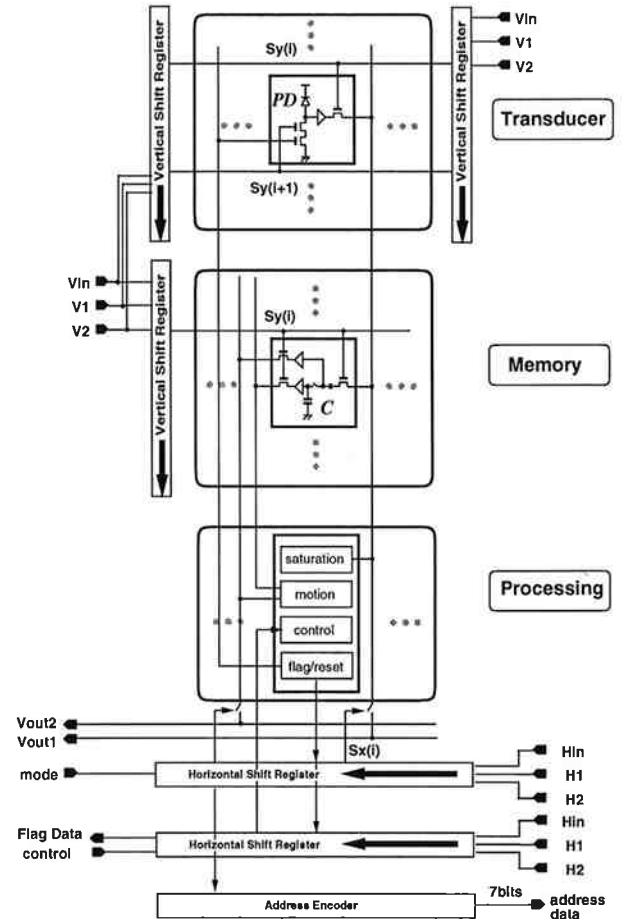


Figure 2: Block diagram of new prototype

architecture. Each pixel has a transducer element and a separate memory.  $V_{PD}(t-1)$  and  $\Delta V_{PD\_last}$  are kept in each memory element and  $\Delta V_{PD}$  is calculated in the memory. The processing element consists of the other circuits to control both integration time and output timing.

### 4. PROTOTYPE CHIP

We prototyped the new adaptive-integration-time sensor by using 2-poly 2-metal  $0.8\mu\text{m}$  CMOS process. Figure 5 shows a layout design of the prototype and Figure 6 shows a packaged chip. Table 1 shows the outline of the prototypes. Pixel pitch, fill factor and processing speed are much improved in comparison with the first prototype.

Table 1: Comparison between first and second prototypes

	first prototype	new prototype
number of pixels	32 × 32	128 × 64
chip size[mm <sup>2</sup> ]	4.0 × 6.1	3.8 × 9.5
element size		
transducer [μm <sup>2</sup> ]	85 × 85	22 × 22
memory [μm <sup>2</sup> ]	85 × 46	22 × 99.3
processing [μm <sup>2</sup> ]	85 × 191	22 × 417
number of transistors		
transducer[trs./pixel]	17	4
memory[trs./pixel]	10	18
processing [trs./column]	64	88
fill factor[%]	14.0	20.2
processing speed[μs / row]	≥ 2	≥ 0.5

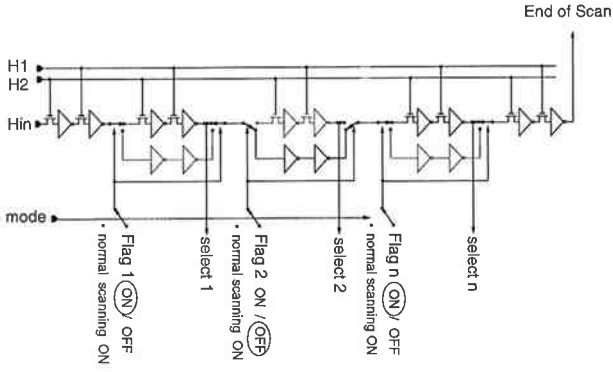


Figure 3: Smart horizontal shift register

## 5. CONCLUSION

In this paper, we present a new adaptive integration time image sensor. The proposed sensor has the circuits for detecting moving and saturated pixels and is able to control both integration time and output timing pixel by pixel. There are some imaging styles by any combination of two flags and external signal.

We describe the circuit design and layout of the prototype which has computational elements based on the column-parallel architecture.

The prototype is now under experiment. Some experimental results of the prototype will be shown in the conference.

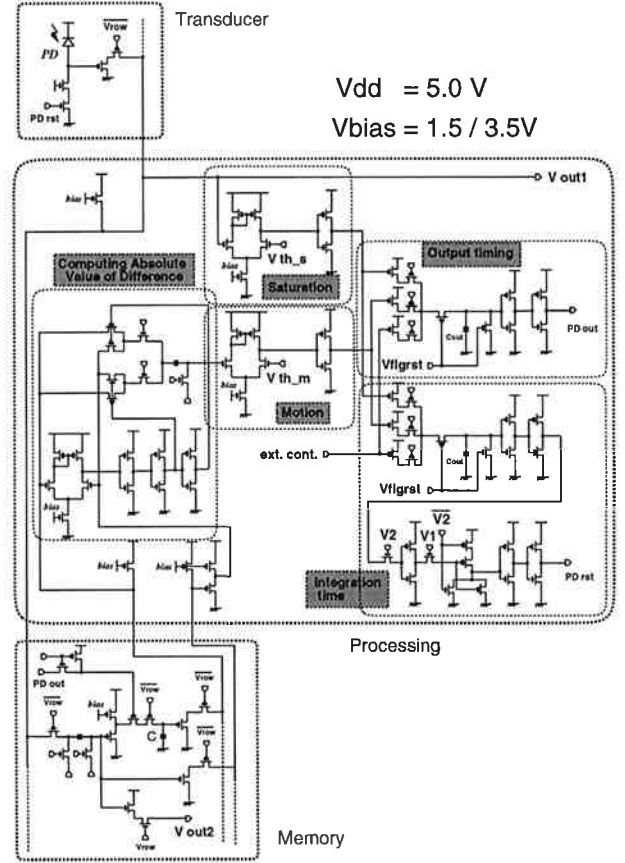


Figure 4: An analog circuit designed for a pixel of the proposed sensor

## 6. REFERENCES

- [1] F.Ando, "Multi-functional Solid State Imaging Techniques" *ITEJ*, Vol.44, No.2, pp. 127-131, 1990.
- [2] T.Hamamoto, K.Aizawa, M.Hatori, "Motion adaptive image sensor", *IEEE Workshop on CCD and Advanced Image Sensors*, R30 (1997)
- [3] K.Aizawa, H.Ohno, Y.Egi, T.Hamamoto, M.Hatori and J.Yamazaki, "On Sensor Video Compression", *IEEE Workshop on CCD and Advanced Image Sensors* (1995)
- [4] K.Aizawa, T.Hamamoto, Y.Ohtsuka, M.Hatori and M.Abe, "Pixel Parallel and Column Parallel Architectures and their Implementations of On Sensor Image Compression", *IEEE Workshop on CCD and Advanced Image Sensors*, R31 (1997)
- [5] T.Hamamoto, Y.Ohtsuka, K.Aizawa, "128x128 pixels image sensor for on-sensor-compression", *IEEE ICIP'98*, Vol.1, pp.493-497 (1998-10)

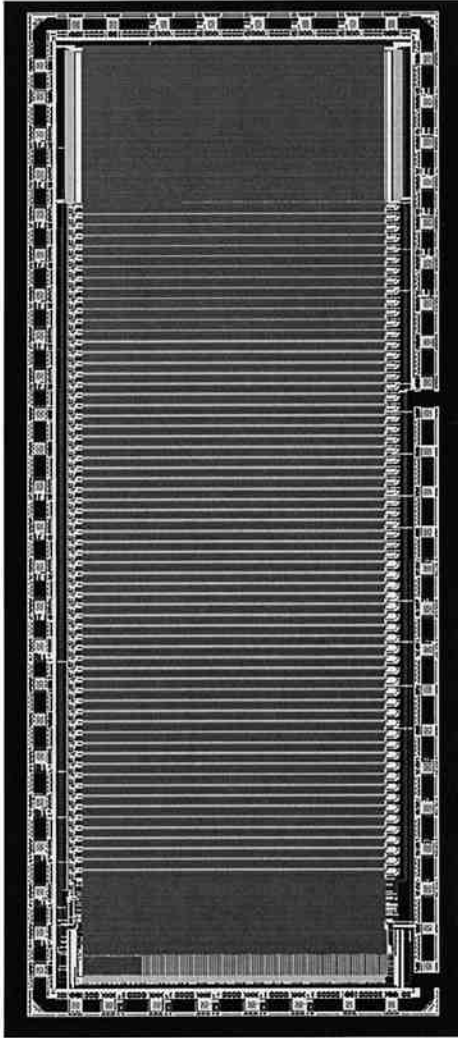


Figure 5: Layout of the prototype

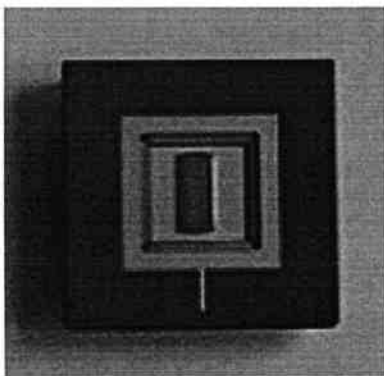


Figure 6: Prototype chip