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Spatially Variant Flexible Sampling Control Integrated on a Sensor Focal Plane

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Abstract

We propose a new sampling control system integrated on an image sensor. Contrary to the conventional random access pixels, the proposed sensor is able to read out spatially variant pixels at high speed, without inputting pixel address for each access. The sampling positions can be changed dynamically by rewriting the sampling position memory. Since the proposed sensor has a array memory that keeps the pixel position to be sampled. The sampling position can be dynamically changed by rewriting the memory array. It can achieve any spatially varying sampling patterns. We have made a first prototype and show results obtained by the prototype.

1 Introduction

In biological vision, the retina is the imaging sensor. It is organized into a space-variant sampling structure including a high-resolution small central fovea and a periphery whose resolution linearly decreases in steps. By this characteristic, it able to centralize and distribute the processing tasks in the earliest stage of vision.

Therefore it is essential for smart sensing to integrate functions of spatially variant flexible sampling control system onto a sensor. The integration on the sensor focal plane will result in dramatical enhancement of performance of the whole image processing systems.

In this paper, we propose a new space-variant sampling system integrated on the sensor focal plane. We will present the principles, circuit designs, a prototype of the sensor and results obtained by the prototype.

2 Spatially Variant Sampling

Spatially variant sampling is a strategy for image acquisition that has been demonstrated to be very interesting for image processing. Traditional machine vision applications have often been hampered by the need of processing huge amounts of data, because they cannot extract only the information required to accomplish specific tasks. It is essential to the vision systems to have specific mechanisms for data reduction and selection that plays major role to simplify visual computation.

Spatially variant sampling allows to select among visual data the relevant information and ignore irrelevant details to the vision systems. This strategy allows a data reduction that has a direct impact on the system performance, especially speed, and on the complexity of the computer architecture to process the image and it is crucial when a real time performance is required.

3 Flexible Sampling Control On An Image Sensor

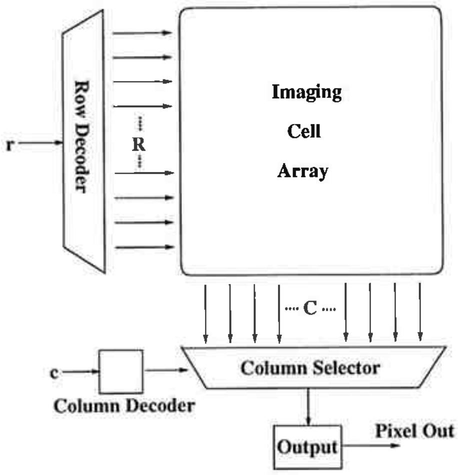


Figure 1: Random Access PD-array.

One of the previous approaches to space variant sampling is random access pixels. For example, there has been an investigation into random access PD-Array sensor[1]. In this sensor, feeding of the pixel address is always needed. Only a single pixel is selected at each access and address of each pixel must be given to read it out. After decoding of each input address by a Row Decoder and a Column Decoder, the corresponding pixel value is read out. Because it needs pixel address for every access, high speed access is difficult.

There has been also an investigation into controlling the access by row or column unit[2]. In this case, it reads out pixel values in blocks or in regular subsampling pattern. Arbitrary control of space-variant control is not possible.

There has been a polar coordinate sensor which has a retina-like sampling positions[3]. It consists of a central high resolution sensor(fovea) and a peripheral sensor, the resolution of which decreases away from the center. Because the sampling positions are geometrically fixed, it is not able to change them.

In this paper a new space variant sampling control which uses sampling position memory is proposed. Each element of the sampling position memory corresponds to each pixel and it contains a binary data to determine the pixel is read out. Thus there is no need to input pixel address for each access, and pixel value can be read out at high speed. Fig.3 illustrates a diagram of the sensor.

A smart scanning shift register (Fig.2) [4] is used to selectively read out pixel values, and the binary data of the memory is used as a control signal to the register. Examples of the read out mode are illustrated in Fig.4 and Fig.5. Subsampling or block access(Fig.4) are easily available. By the smart scanning, only those pixels, the memory elements of which are H, are read out in a compact sequence. the pixels, the memory of which are L, are immediately skipped. Sampling at high resolution at center and low resolution at peripheral pixels, similar to foveated vision(Fig.5), are also available. Fig.5 is the images obtained by the simulation. The left is the original image and the right is the simulated image consists of center portion at normal resolution(128pixel radius) and peripheral radially subsampled.

By rewriting the sampling position memory, the position of the fovea can be freely moved on the sensor. Therefore if we use the sensor in active vision systems, the fast feature extraction is possible.

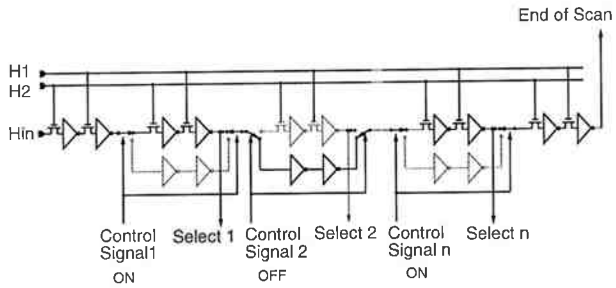


Figure 2: Smart scanning shift register.

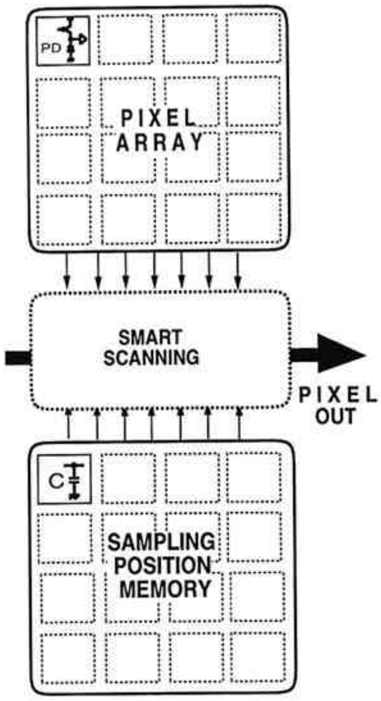


Figure 3: Diagram of sampling control system.

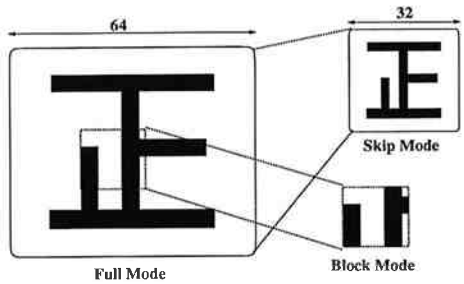


Figure 4: Block and skip access mode.

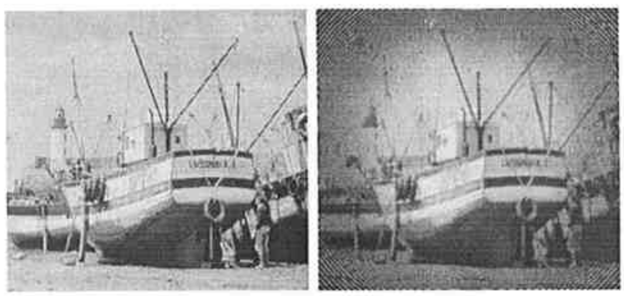


Figure 5: Fovea-like output image.

4 Circuit Design of A Prototype

Fig.7 shows the block diagram of the sampling control sensor. This sensor mainly consists of two parts. They are pixel array and sampling position memory. Fig.6 shows an analog circuit of the pixel and the memory.

Pixel array consists of pixel circuits. A pixel circuit consists of a few transistors, so that we can get a practical fill factor. Pixel values are transmitted to the horizontal shift register, and selected based on memory values of sampling position memory. And values of only the selected pixels are read out.

The proposed sensor has two different type of horizontal shift registers: a normal and a smart scanning shift registers. One of the two is selected by the mode selection signal. In the case of the smart scanning shift register, only the selected pixels are read out and non-selected pixels are skipped without reading. In order to reconstruct the output image, address data is required, wherein known sampling position may be used.

Sampling position memory mainly consists of a capacitance and switches and can be dynamically rewritten.

Both pixel array and sampling position memory have vertical shift registers which are driven by the same signals to select corresponding pair of rows. The sensor has another horizontal shift register at the bottom so that it can rewrite independently sampling position memory within a horizontal scanning period.

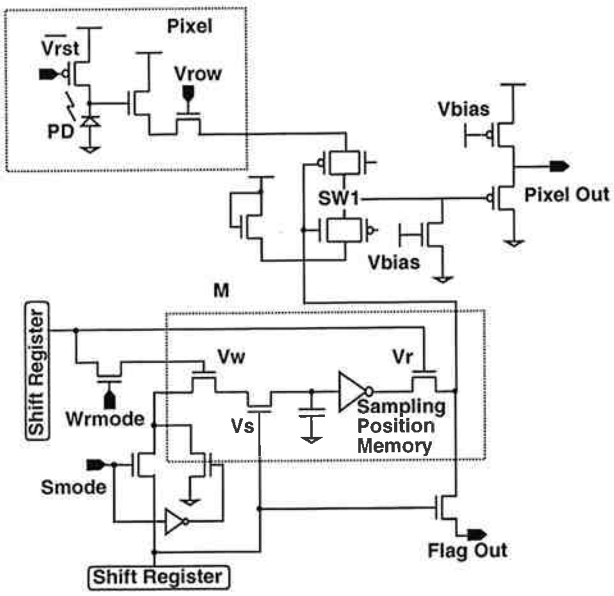


Figure 6: A design of pixel circuit and sampling position memory.

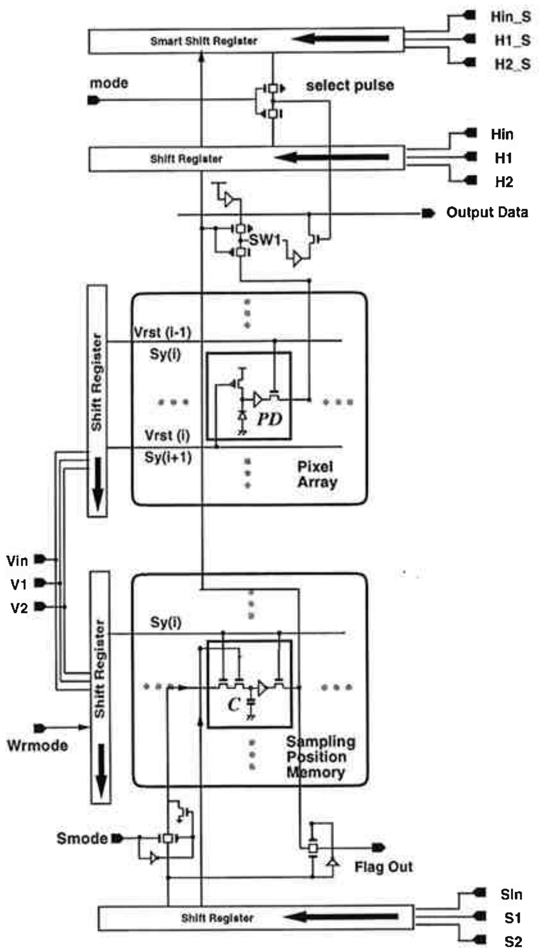


Figure 7: Block diagram of sampling control image sensor.

The bottom horizontal shift register can also read out the control bits as flag signals.

In order to write control bits in sampling position memory, the output signal from the horizontal shift register is controlled by sample selection signal (*Smode*). If *Smode* is "1", the output signal from the bottom shift register is transmitted to the memory and its value is set to "1". If *Smode* is "0", the memory is reset. Using *wrmode* signal, the signal from shift register is input only at the time of writing.

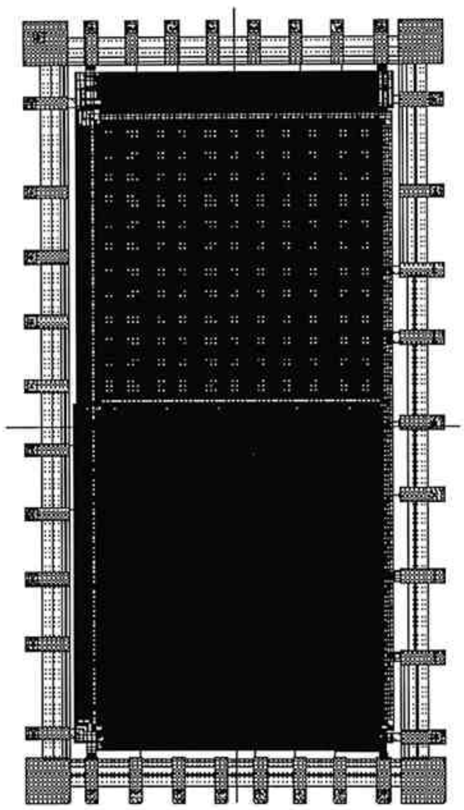


Figure 8: Chip layout of a prototype.

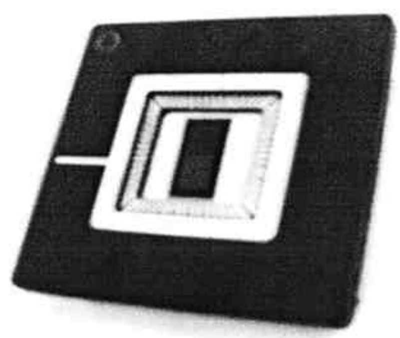


Figure 9: A prototype chip.

5 A Prototype Chip

Fig.8 shows a chip layout of a prototype, and Fig.9 shows a picture of the prototype chip. Table 1 shows

Table 1: Characteristics of the prototype.

♯ of pixels	64 × 64 pixels
♯ of transistors	pixel : 3 trs. / pixel memory : 9 trs. / pixel
fill factor	25%
power dissipation	5mW / chip

the characteristics of it. It is designed under 1-poly 2-metal CMOS 0.7μm rule. Table 1 shows the characteristics of the prototype. The number of the transistors in the pixel array element is three, which is equal to the conventional CMOS sensor [5]. Number of pixels is 64 × 64.

Figure 10: An image obtained by the prototype.

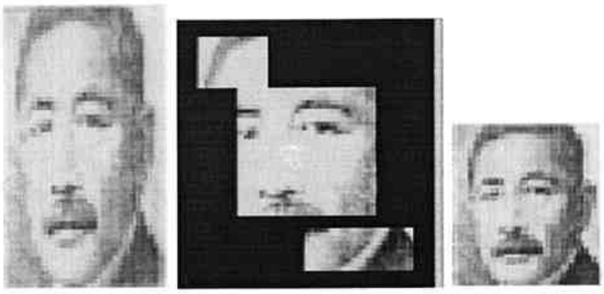


Figure 11: Output images selectively sampled by the prototype.

Fig.10 shows an output image obtained by the prototype. Fig.11 shows images obtained by the prototype in skip or block access mode. The left is the image when every other column is sampled and read out by the smart horizontal shift register. The right is the one when every other column and every other row is sampled. The center is the one when specific block areas are selectively sampled. The skipped pixels are shown black.

Fig.12 shows two examples of the varieties of sample-controlled image. The left images are obtained by the prototype at smart scanning mode. The center images are the flag data in the sampling position memory. The right are reconstructed images, among the two examples, (b)shows a retina like sampling where the density changes high to low from the center to the peripheral.

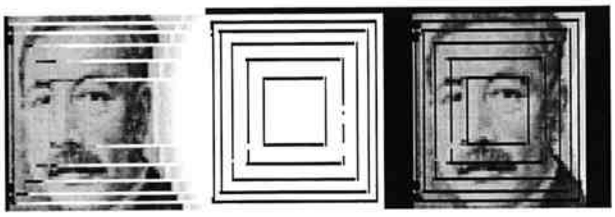
6 Conclusions

Proposed is a new image sensor with space-variant flexible sampling control integrated on a sensor focal plane. The principles of the processing, the designs of the circuits based on column parallel architecture, and the prototype chip have been presented.

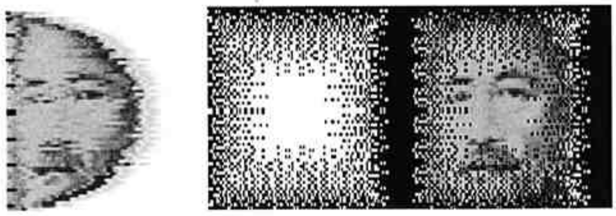
The following advantages is obtained from the sensor.

- It can set arbitrary sampling positions.
- Sampling such as high resolution at center and low resolution at peripheral pixels, similar to foveated vision, is available.
- It can also output in blocks or by regular subsampling patterns.

The prototype is now under further experiments in a system that enables it to dramatically control spatially variant sampling pattern and time-resolution radially for retina-like sensing.



(a)



(b)

Figure 12: Two examples of varieties of the sampled image. (b)is retina-like sampling.

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