R7 A 1/3" VGA CMOS Imaging System On a Chip

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Abstract

A significant number of advances have been reported in CMOS imagers in the recent past [1,2]. Amongst the advantages that CMOS imagers offer, the ability to integrate functions of a multitude of chips into one, stands out. The ultimate goal remains the realization of a "system on a chip (SOC)" that is suitable for high volume applications with lower cost and power dissipation while remaining competitive in electro-optical performance with CCDs. Widely reported issues with CMOS imagers include poor sensitivity and dynamic range [3]. Described in this paper is the performance of a CMOS imager developed by Motorola that integrates the functionality of a complete analog image acquisition, digitizer, and digital signal processing system on a single chip. The SOC delivers extremely good performance including a very high system dynamic range and sensitivity.

Introduction

The 1/3", VGA resolution, active pixel imager is fabricated on a 0.5μm/3.3V twin-well, three layer metal CMOS process. With the exception of two additional masks for the pinned photodiode pixel element and a second polysilicon layer for analog functions, the standard production CMOS process is used. The photoelements based on 7.8x7.8μm^2 active pixels, utilize a 4-transistor architecture. The pinned photodiode allows improved blue response, lower dark noise and a lag free pixel operation[4].

The on-chip image processing engine includes a bank of programmable gain amplifiers, line rate clamping for dark offset removal, real time auto white balancing, per column gain and offset calibration, and a 10 bit pipelined RSD analog to digital converter with a programmable input range. Post ADC signal processing includes features such as bad pixel replacement based on user defined threshold levels, 10 to 8 bit companding and 5 tap FIR filtering. The sensor can be programmed via a standard I^{2}C interface. Programmable features include variable frame rates using a constant frequency master clock, electronic exposure control, continuous or single frame capture, progressive or interlace scanning modes. Each pixel is individually addressable allowing region of interest imaging and image sub-sampling.

The sensor operates with a single master clock that can run at frequencies of up to 20MHz. A single 3.3V supply powers the chip. A total programmable gain of 27dB is available. The measured "system on a chip" dynamic range is 50dB thus giving over 8 true bits of resolution. Extremely high conversion gain results in peak sensitivity of 19V/μJ/cm^2 or 3.0V/lux-sec. Total power dissipation is 400mW at the maximum speed of operation.

Image Sensing

The sensing element consists of a 4T cell shown in Figure 2. All pixels in a row have common Reset, Transfer, and Row Select controls. In addition all pixels have common power supply (VDD) and ground (VSS) connections. The use of switched capacitor techniques in the readout column architecture allows the use of capacitor ratios rather than absolute values hence a better control on gain variations thus FPN. The noise performance is also improved since the gain is applied close to the pixel output. Further, the scheme allows a positive pixel gain which in conjunction with an optimally designed floating diffusion of 4fF yields a total charge to voltage conversion gain of 60μV/e. An analog saturation signal of 1300mV peak-to-peak is presented to the input of the analog signal processing chain.

The reset gate also functions as a lateral antiblooming gate. During integration, it is turned ON thus draining any charge that blooms over the transfer gate into the floating diffusion. Optimized geometries for the pixel gates yield a fill factor of 35%. With the use of microlenses this is effectively doubled. Color separation is achieved by patterning RGB-Bayer monolithic polymer Color Filter Arrays (CFAs).

The pixels have electronic exposure which can be controlled in steps of 1x to 1/256x of a given frame readout time. The sensor allows frame capture in two modes. The continuous or rolling frame capture which is commonly seen on CMOS sensors, integrates one row at a time. In some ways it is similar to the Time Delay and Integration (TDI) operation of a CCD. Frame rates of over 50/sec can be achieved at 20MHz operation of the sensor. Still Frame capture is similar in operation to most shuttered area CCDs. An entire frame is captured then read out line by line. Frame rates are dominated by the frame readout time in this case. In addition, image scanning can be done in progressive or interlace modes. Additional frame rate control is available by adding redundant clocks at the end of each line or adding redundant lines at the end of each frame. The start/stop rows and columns can be programmed allowing programmable x-y windowing. Image sub-sampling in 1/1, 1/4, and 1/16 modes is possible.

Image Processing

The image processing chain consists of a line rate clamping circuitry. The pixel dark levels are stored on external sampling capacitors. This is used to establish the black reference level hence corresponding zero ADC code. Dark clamping can be done at line or frame rate using either the dark columns or dark rows.

Three Programmable Gain Amplifiers (PGA) are available. Their gains can be programmed individually from 0.9x-2.8x in 64 steps. The first PGA allows combination of global 'coarse' gain and a column specific 'fine' gain application. An on-chip RAM stores 704 words with 4-bit gain values for each specific column. This function is especially useful for channel to channel gain normalization to further help improve Fixed Pattern Noise (FPN) and Photo Response Nonuniformities (PRNU). The second PGA is used to apply a global gain to all the pixel outputs in the array. And finally the third PGA is used for automatic white balancing. A maximum of four gain coefficients can be preloaded into storage registers. Once loaded, the appropriate gain values are multiplexed via a high speed path and applied to the pixel output at the readout speed. Another unique feature is the automatic column offset correction. As with the column gain PGA, a 'coarse' global and a 'fine' per column offset adjust is possible. An on-chip RAM can be loaded with 704, 4 bit signed words to allow per column offset adjust. Column offset values can also be loaded automatically by allowing the sensor to scan its dark rows. All pixels are compared against reference pixel. The difference is determined and stored on the RAM and subsequently added to the global offset level to give a full range of +/-128LSBs offsets.

A pipelined, redundant signed digit algorithmic technique incorporating digital error correction is used to yield a 10-bit ADC with superior characteristics for imaging applications. A programmable voltage reference generator allows setting the ADC's input dynamic range anywhere from 0 to 2.5V. This programmable feature can be used in addition to available PGAs and offset adjust blocks to maximize dynamic range.

Post analog signal processing circuitry allows bad pixel replacement, data companding, and FIR filtering. The user can set threshold levels for dark and bright pixels to detect bad pixels. Pixel outputs beyond these thresholds are replaced by the average pixel values of the same color neighboring pixels. The data compander allows coring of the lower order bits by expanding lower signal levels and compressing high light levels. The companding function performs a 10 to 8 bit transformation on the data. On chip FIR filters allow additional filtering of column noise. The 5 tap, 1-dimensional filter allows for image enhancements by assuming the characteristics of a low or high pass filter depending on the programmed tap ratios.

Conclusions

A high performance active pixels based CMOS imager has been successfully developed and characterized. The imager integrates a number of unique imaging functions making it truly a complete system on a chip. The reported device has excellent sensitivity and dynamic range. Given the high frame rate, low power, and good performance it is suitable for both consumer and industrial applications.

References

[1] Wong, H-S "CMOS Image Sensors – Recent Advances and Device Scaling Considerations", IEDM Technical Digest 1997

[2] Hogan, H. "Image is Everything", Photonics Spectra, Dec 1998, pp82-88

[3] Fossum, E. "CMOS Image Sensors: Electronic Camera On a Chip", IEDM Technical Digest, 1995 p.17-25

[4] Guidash, R.M. et al "A 0.6μm CMOS Pinned Photodiode Color Imager Technology", IEDM Technical Digest, 1997, p.927-929

Table 1. Performance Specifications

Parameter	Value
Resolution	640x480
Pixel Size	7.8 μm x 7.8 μm
Fill Factor	35%
Peak Responsivity	19V/μJ/cm² (3.0V/Lux-Sec)
Peak QE	17%
Saturation Equivalent Exposure	0.14μJ/cm²
Photo Response Non Uniformity	2% rms
Dark Current	0.5-2nA/cm²
Programmable Gain	-2.7dB to 27dB
Data Output	10 bit linear/ 8-bit companded
"System" Dynamic Range	50dB (>8 bits)
Readout Rate	20MHz
Frame Rate	52FPS
Power Dissipation	400mW
Die Size	7500μm x 7200μm
Package	48 pin CLCC

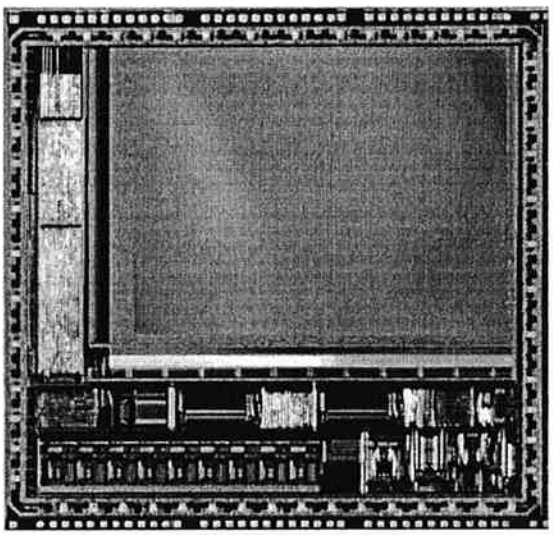

Figure 1. Chip photomicrograph

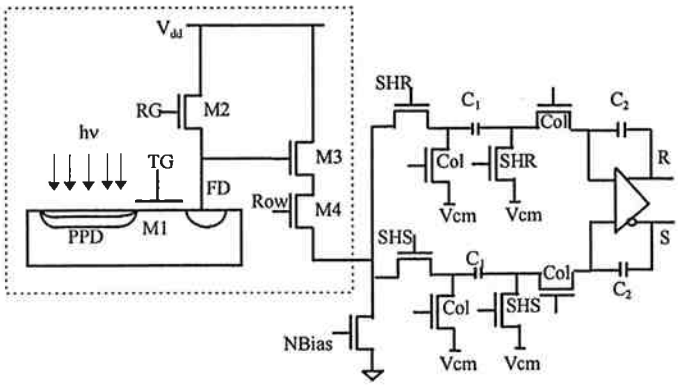

Figure 2. Pixel and readout column

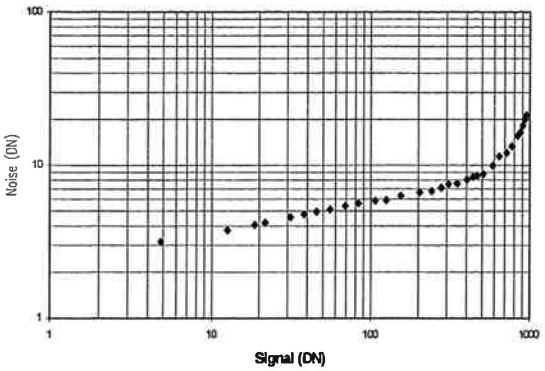

Figure 3. Photon transfer curve for the system yields a dynamic range of 50dB

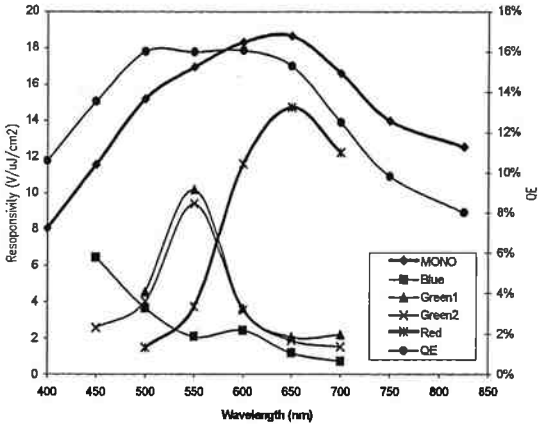

Figure 4. Monochrome and color responsivity

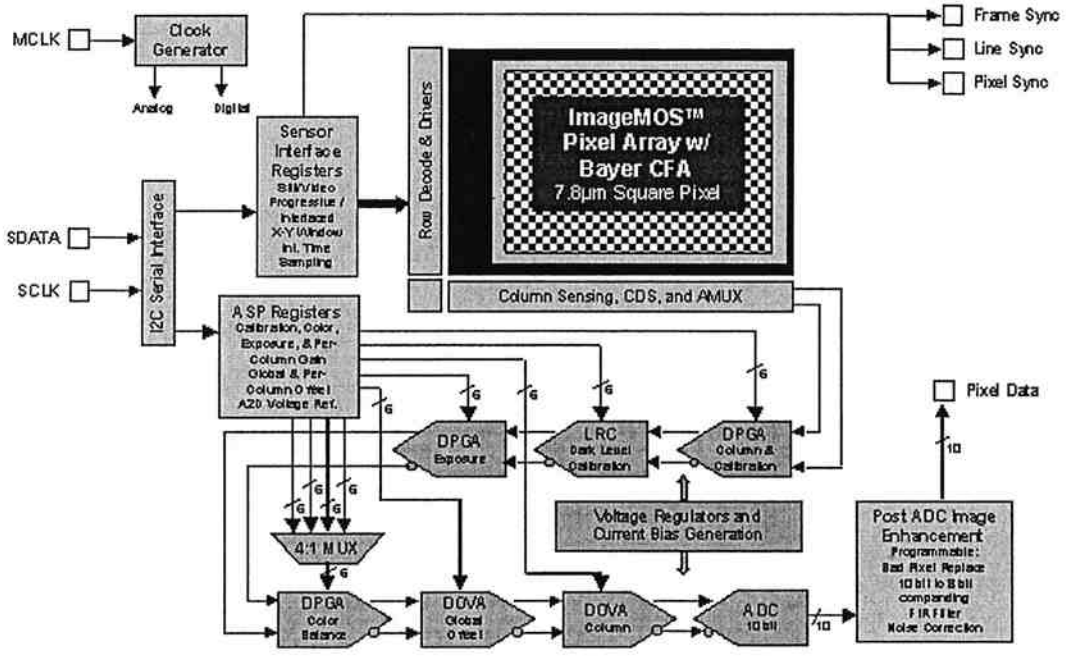

Figure 5. System architecture