

## 256 x 256 Pixel CMOS Imager with Linear Readout and 120dB Dynamic Range

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### Abstract

In this contribution, a 256 \* 256 pixel CMOS imager is described, which features linear readout, 120dB dynamic range (DR), 56dB signal-to-noise ratio, 65% filling factor, and an effective frame rate of 50 Hz. The imager has been integrated in 1 $\mu$ m double-metal CMOS technology. Sample images exhibiting high DR are presented and compared to those taken with a conventional CCD imager.

### 1. Introduction

It is well known that the human vision system exhibits an enormous optical dynamic range (DR about 200dB), as it can adapt to an extremely high range of light intensity levels [1]. Artificial imagers compare poorly with the human eye: conventional CCD imagers exhibit usually a DR of only about 50-70dB. CMOS imagers that employ logarithmic readout achieve higher DR (up to 140dB), but they suffer from the loss of contrast and increase of noise [2, 3]. Also, all these devices do not allow any local "brightness" adaption. It is interesting to note that most display devices, e.g. CRTs, have also low DR, i.e. 30-40dB typically.

In this contribution a CMOS imager is presented, that combines a DR of almost 120dB with linear readout

capability. This ensures excellent contrast and noise properties. Although it is feasible to design CMOS imagers with purely local on-chip brightness adaption [4], the design and implementation presented in this paper combines pixel-local circuitry with off-chip brightness processing to achieve the effective 120dB intensity range individually for each pixel. This was done, in order to avoid deterioration of both: contrast quality and of signal-to-noise ratio (SNR).

### 2. Circuit description

The pixel design is based on integrating photodiodes formed by an n<sup>+</sup>-diffusion in a p-substrate [5]. The photo diodes are periodically reset and the discharge voltage caused by the photo current is sensed using a source-follower (see Fig. 1). Each pixel signal is available at the corresponding column line of the pixel matrix.

The column readout employs a switched-capacitor (SC) precision amplifier buffered by an output source follower. Each SC amplifier allows time-multiplexed cyclical access to all row pixels of a column. The operational amplifier used in the SC circuit is based on a folded cascode structure with a low-voltage cascode at the output. Correlated double sampling operation (CDS) is employed for each pixel readout operation, in order to

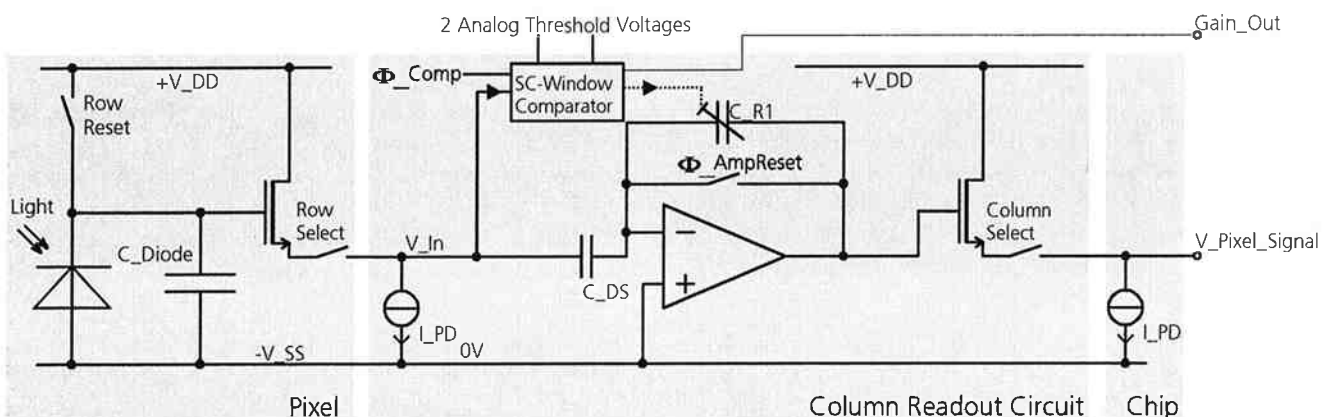


Fig. 1: Simplified schematic of pixel and column readout circuits

reduce fixed pattern noise (FPN), low frequency random noise, and the offset. The pixel CDS is always applied with respect to the reset signal of the subsequent frame (rather than with respect to the previous reset signal, see Fig. 2): this yields minimum correlation time for low photocurrents and thus provides the best 1/f-noise reduction, especially at low irradiance levels.

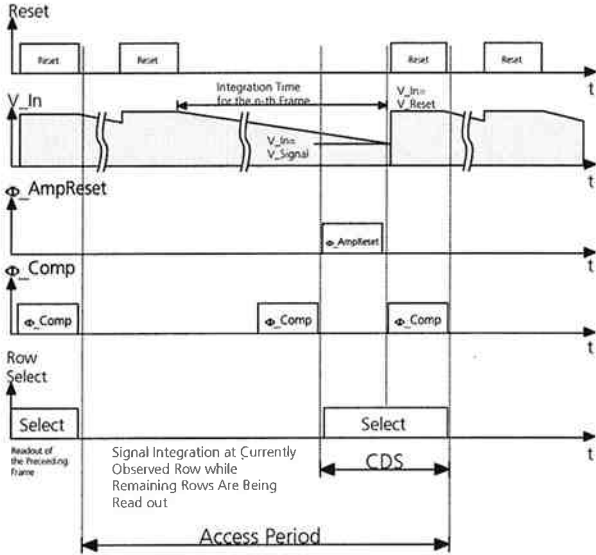


Fig. 2: Timing diagram for a single pixel

Fig. 3 depicts a simplified version of the chip architecture.

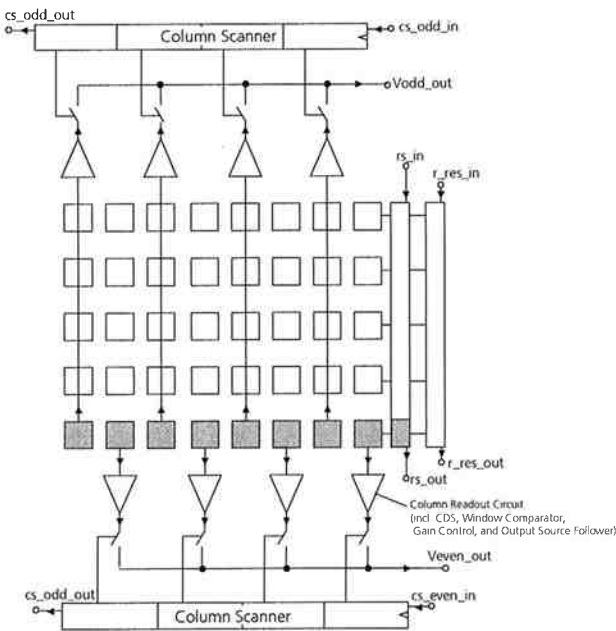


Fig. 3: Architecture of the CMOS imager

### 3. High dynamic range technique

Within the time interval of a single frame, each pixel can be multiple-accessed: this allows "exposure" with up to four different integration times. For each pixel the imager electronics subsequently selects the optimum integration time interval, i.e. the longest interval during which the output of the column amplifier has not yet reached the saturation voltage level. The optimum integration time is chosen for each pixel individually, and the resulting pixel-specific time-code (2-bit) is stored in an off-chip frame memory.

In addition, the gain factor of the column SC amplifier is adapted appropriately. Since each column amplifier is equipped with a variable voltage gain that can be digitally controlled by a window comparator, an automatic pixel-specific adjustment of the amplification factor with respect to the relevant signal level is applied (3 different gains are available). The gain information is also stored as 2-bit code in the frame memory and thus constitutes supplementary information about the relevant pixel signal. For the windowing, two distinct thresholds are utilized with appropriate window overlaps in order to avoid offset and noise problems at the boundaries. The amplified pixel signal is available at the output of the source follower that buffers the column SC amplifier.

The output signal is then externally A/D-converted, and the resulting 10-bit value is finally stored in the frame memory, too. All these operations are carried out for each pixel in each frame individually. Absolutely no information from preceding frames is being used. While the pixels of each column are accessed sequentially, the column amplifiers operate all in parallel. Therefore, the readout time for all pixels of one column determines the minimum frame period (see Figs. 2 and 3).

The pixel brightness information finally stored in the frame memory is thus composed of three distinct values: (i) the selected integration time, (ii) the selected gain, and (iii) the digitized pixel voltage signal. This 14 bit composite data represent an equivalent of 20 bit linear resolution for the pixel intensity value, which corresponds to a 120dB range. The 20-bit linear intensity signal can be easily computed by utilizing an appropriate 14-bit look-up table (LUT). Under irradiance the photon shot noise increases at higher intensity levels; therefore, a nonlinear distribution (a square-root dependence to be precise) for the integration times and voltage gains has been employed.

### 4. Experimental results

The CMOS imager presented in this work has been implemented in 1 $\mu$ m double-metal CMOS technology. The chip features 256 \* 256 pixels (filling factor: 65%). Including control and readout electronics it occupies a

die area of 90.9mm<sup>2</sup> (see Fig. 4) and consumes 80mA (at 5V voltage supply and 4.2MHz pixel clock frequency).

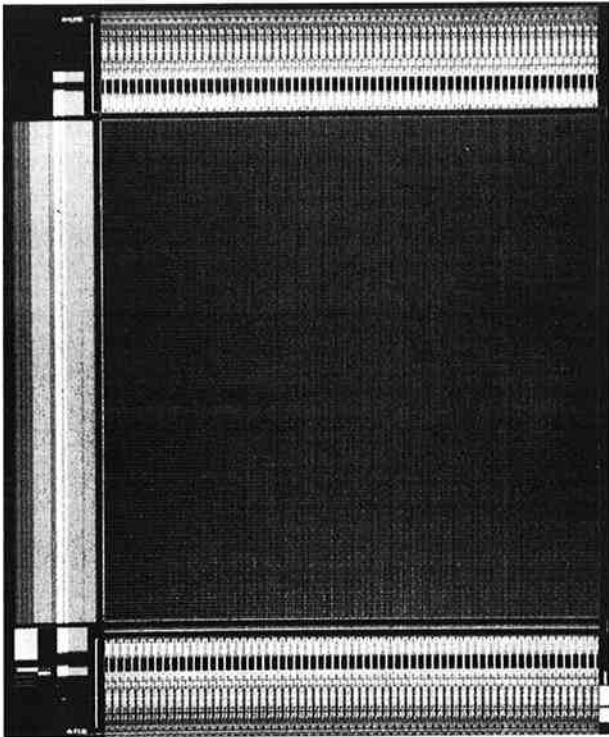


Fig. 4: Chip photomicrograph

The multiple pixel access allows to select between 1, 2, or 4 integration times per frame period. With a single integration interval, the readout time is 5ms. However, since 4 pixel readouts are required per image, the effective frame rate amounts then only to 50Hz (including all operations required for full gray level linearization).

Measurements at room temperature yielded a signal-to-noise ratio (SNR) due to FPN of 52dB, a temporal SNR of 56dB, and a global DR of 118.7dB, provided that the voltages of all 4 integration time intervals per frame are being sampled. Application of only 2 integration samplings per frame yields still a global dynamic range of 103dB, but provides the effective frame rate of 100Hz. When only a single integration time is used, the DR decreases to only 71dB, while the effective frame rate is sped up to fast 200Hz. Since the

clock frequency of the imager can be externally controlled, the camera can be also operated at lower pixel frequencies: at 1.05MHz clock frequency and 50 frames/s the maximum light sensitivity is obtained when a single integration time of 20ms is applied. In Fig. 5 the measured pixel output for 2 integration times and 3 voltage gains is depicted as a function of the input light intensity.

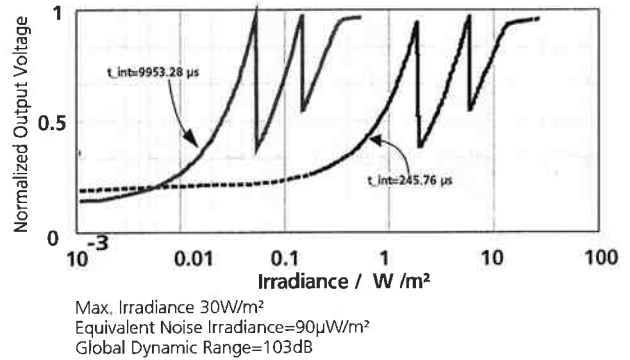


Fig. 5: Measured pixel characteristics (shown for 2 different integration times and 3 voltage gains)

The imager has been also tested at increased temperatures. At 65 °C no loss of image quality was observed; at 85 °C the decrease of DR amounted to only 10dB.

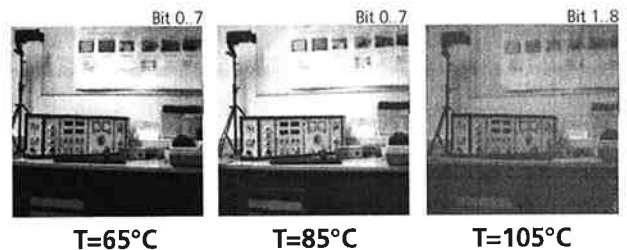


Fig. 6a, 6b, 6c: Images at 65°C, 85°C, and 105°C (images recorded without FPN cancellation)

For demonstration purposes, the full linear gray level information of each composed pixel signal stored in the frame memory is expanded to 20 bits for display on a CRT screen.

Figs. 7a-7c show different linearized gray level ranges of a single lab scene, which have all been taken from an



Figs. 7a, 7b, 7c: Different gray levels displayed (out of total of 20 bits that belong to the identical image)

identical image. In order to highlight the excellent DR and SNR properties of the imager, extremely inhomogeneous single-frame illumination has been applied to the scene. Because of the limited global DR of the CRT display, only a limited number of pixel gray values 256 (rather than a million) can be displayed at a time.

Fig. 8 visualizes another aspect of the relevant sample image, featuring a gray level compression scheme based on spatial bandpass filtering. This transforms the 20-bit pixel values to the appropriate range of 8-bit screen display values, while it essentially preserves brightness-normalized contrast. Obviously, this transformation corresponds to a local brightness adaption, which has been applied here to overcome the limited global DR of the display. For the sake of visual comparison, an image of the identical lab scene was taken with a commercial CCD camera; the corresponding image is depicted in Fig. 9.

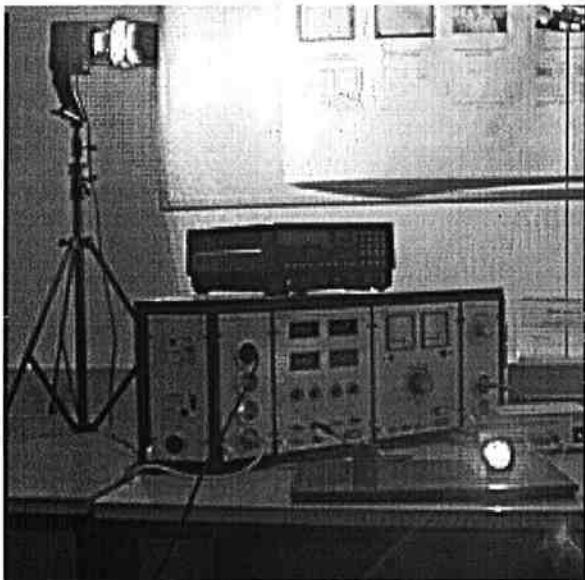


Fig. 8: The same image as in Figs. 7a-7c taken with our CMOS imager (iris fully open). Using a spatial bandpass the 20 bit linear signal has been compressed to amplitude resolution of 8 bit while preserving normalized local contrast.

### 3. Summary

A 256 \* 256 pixel array CMOS image sensor has been presented. It delivers an excellent image due to its linear readout but an additional pixel signal processing yields a 120 dB dynamic range at video rates until now reserved for CMOS camera with logarithmic readout.

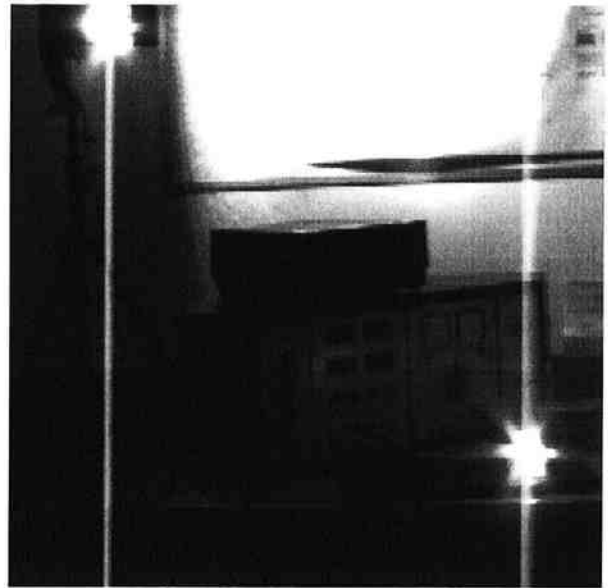


Fig. 9: The same image as in Figs. 7a-7c, and 8 but taken using a conventional CCD imager at the smallest possible iris opening.

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