R3: Influence of Sensor Settings and Doping Profile on Dark Current in FT-CCD's

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Abstract

Dark current generation in FT-CCD's strongly depends on the electric fields close to the surface and at the junction between the p+ channel stop and the n-channel. Reduction of these electric fields can be achieved by increasing the voltage on the channel stops. However, due to surface pinning this will lead to lower charge handling capacity and lower sensitivity. Pinning can be avoided by changing the doping profile. Therefore, we have performed device simulations using a method for automated optimisation of FT-CCD's. From these simulations we found that we have to increase the n-channel top dope. The simulation results are implemented in new devices. Evaluation of these devices shows a decrease of dark current of 28% at the expense of a decrease of the maximum charge handling capacity of about 48%. The sensitivity remains the same.

Introduction

The dark current of an image sensor is a very important characteristic. Lowering the dark current will improve the dynamic range due to a reduction of the shot noise on the dark current. Furthermore, dark current reduction is correlated with a decrease of the fixed pattern noise and a reduction of the amount of white pixels in dark.

In this paper we will focus on the optimisation of the adjusted voltage settings of FT-CCD's for dark current reduction. The dependence of the dark current on the applied voltages is caused by the fact that the dark current generation strongly depends on the electric field [1]. We have studied this dependence by 3D off-state device simulations and evaluation of a VGA imager (640(H) × 480(V) pixels) with 5.1 × 5.1 μm^2 pixels made in double membrane poly-Si technology as reported in [2] but with the conventional doping profile for vertical antiblooming [3].

Reduction of electric field

Figure 1 shows results of a 3D off-state device simulation of the electric field (contour lines) in a pixel. The highest electric field is located close to the surface at the junction between the p+ channel stop and the n-channel. To reduce this electric field and thereby suppress the dark current generation the voltage on the channel stops (Vps) should be as high as possible. Figure 2 shows that an increase of Vps from 3V to 5V results in a dark current reduction of 35%.

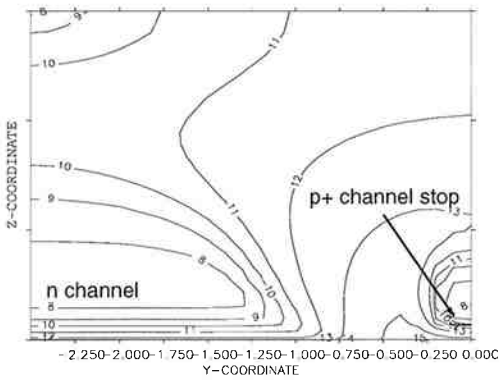

Figure 1: Cross section of half a pixel perpendicular to the transport direction showing the electric field contour lines. The highest electric field (highest number) is located close to the surface at the junction between the channel stop and the n channel.

However, from the evaluation of several devices it turned out that for Vps>3V a higher Vps results in a higher substrate voltage (Vns) necessary for correct antiblooming (figure 3). This is shown in figure 3 where Vns and the maximum charge handling capacity (Qmax) are plotted. Such an unconventional Vps-Vns dependence is caused by surface pinning under the blocking gates.

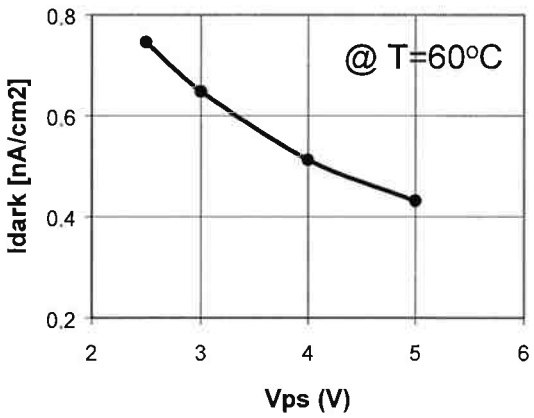

Figure 2: Dark current versus Vps. An increase of Vps results in a decrease of Idark.

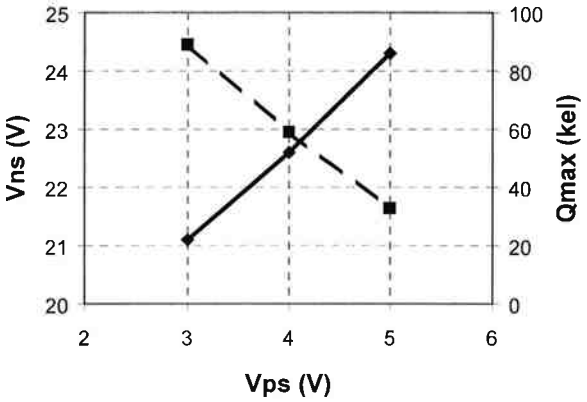

Figure 3: Substrate voltage (full line) and full-well capacity (dashed line) versus Vps. The Vns-Vps dependence is caused by pinning. An increase of Vns results in a decrease of Qmax.

Figure 4 shows the results of a device simulation of the hole concentration at the surface, showing a high concentration under blocking gates. Due to pinning the channel potential under the blocking gates will increase with increasing Vps. This will lead to a lower lateral barrier which results in a higher Vns for correct antiblooming (see figure 5).

Automated optimisation

Pinning at Vps=5V can be avoided by changing the doping profile. Of course, this will also change other sensor parameters. To find a suitable doping profile meeting this non-pinning condition, we have performed device simulations. We have used the method for automated optimisation of FT-CCD pixels as reported in [4] with a set of four input parameters: p-well top dope (DPTOP), n-channel top dope (DNTOP), Vps and Vns. Each of these parameters is varied over a certain range in 4 to 6 steps. The number of electrons in the pixel is set by adjusting the quasi Fermi level to the point where the vertical anti-blooming barrier is about 0.4 Volts [3]. Eight output variables are extracted, like: the number of electrons in a fully filled pixel (Qmax), the collection depth of the pixel (z_min), the lateral barrier (Vbarl) and the surface potential under a blocking gate (pot_sur). In figure 6 pot_sur, Vbarl, Qmax and z_min are shown as 2D cross sections of the 4D input parameter space.

Figure 6a shows the surface potential under a blocking gate as function of DNTOP and Vns for Vps=5V. We can see that for 19V ≤ Vns ≤ 26V the surface is pinned for DNTOP < $2.1 \cdot 10^{22}$ m^{-3}. So, to meet the non-pinning condition for Vps=5V we have to increase DNTOP considerably. In figure 6b the lateral barrier is shown in the same cross section. From this graph we see that an increase of DNTOP will lead to an increase of Vns if the lateral barrier is kept constant. Figure 6c shows that a higher Vns will lead to a lower Qmax. The collection depth of the pixel will decrease with Vns but will increase with DNTOP as can be seen in figure 6d. An increase of z_min will directly influence the sensitivity. The simulation results are summarised in table 1.

Experiments

Various n-channel top dopes are implemented in new devices, which have been evaluated. In table 1 the experimental results are compared with the simulation results. From the measurements it turns out that the devices with a DNTOP of 2.2E22 m^{-3} get into pinning for Vps>4.7V. Therefore, the evaluation of the devices has been done at a 0.5V lower Vps than the simulations. Furthermore, we found that the Vns necessary for correct antiblooming is higher than expected from the simulations. Due to this higher Vns the predicted sensitivity gain is cancelled out, although the measurements and simulations of Qmax show comparable results. We achieved a decrease in dark current of about 28% at the

expense of a decrease of Qmax of about 48% without a decrease in sensitivity.

The dark current reduction is less than the 35% mentioned before. This can be explained by the increase of the n-channel doping. Increasing the channel implant dose will lead to a higher electric field at the surface above the n-channel. This will cause an increase in dark current generation in this part of the device. However, in spite of this higher channel doping the electric field between the p+ channel stop and the n-channel is decreased. The overall effect on dark current turned out to be positive, which is correlated with a decrease of the fixed pattern noise and a reduction of the amount of white pixels in dark.

Conclusions

Reduction of dark current in FT-CCD's can be achieved by increasing the adjusted voltage on the channel stops. However, it turned out that due to surface pinning a higher substrate voltage is needed for correct antiblooming leading to a lower sensitivity and a lower saturation level. From device simulations we found that we have to increase DNTOP considerably to meet the non-pinning condition for Vps=5V. By changing the doping profile we achieved a dark current reduction of about 28% without changing the sensitivity, but with a decrease of Qmax of about 48%.

References

[1] W.J. Toren, J. Bisschop: "Complete characterization of dark current in frame transfer image sensors", *Philips J. Res.* **48**, 1994, pp. 207-231.

[2] H.L. Peek *et. al.*: "An FT-CCD imager with true 2.4 × 2.4 μm^2 pixels in double membrane poly-Si technology", *IEDM Technical Digest*, 1996, pp. 907-910.

[3] M.J.H. van de Steeg et al.: "A Frame Transfer CCD color imager with vertical antiblooming", *IEEE Trans. Electron Devices* **32**, 1985, pp. 1430-1438.

[4] A. Heringa, J. Bosiers, E. Roks: "Automated optimisation of FT-CCD image pixels", *IEEE Workshop on CCD and AIS*, 1997.

Simulation results						
DNTOP (m^{-3})	Vps (V)	Vns (V)	pot_sur (V)	Qmax (ke^-)	z_min (μm)	
1.4E22	3	21	3.0	73	1.49	
1.8E22	4	23.5	3.9	36	1.56	
2.2E22	5	25	4.7	28	1.62	
Experimental results						
DNTOP (m^{-3})	Vps (V)	Vns (V)		Qmax (ke^-)	Sensitivity [ke^-/lux·sec]	Idark (nA/cm^2) @ T=60°C
1.4E22	2.5	22		67	14.5	0.83
1.8E22	3.5	26		40	14.3	0.75
2.2E22	4.5	28		35	14.5	0.60

Table 1: Comparison of device simulation results with experimental results.

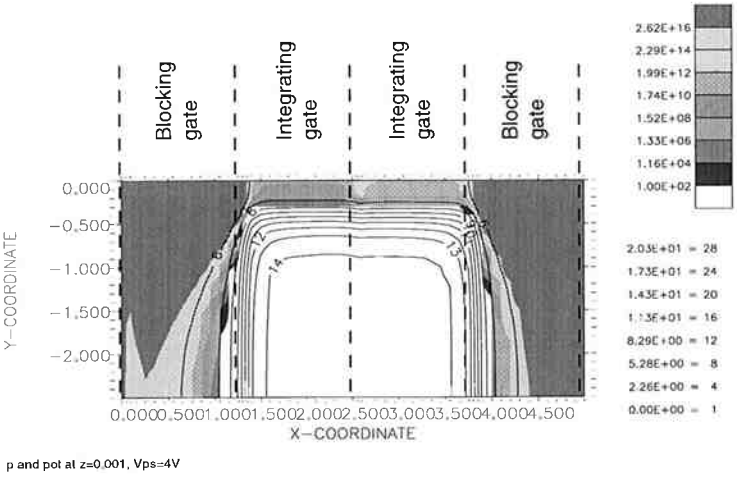

Figure 4: Cross section of half a pixel at the Si-SiO2 interface (top view) with hole concentration (colours) and potential profile (countour lines) showing a high hole concentration under the blocking gates.

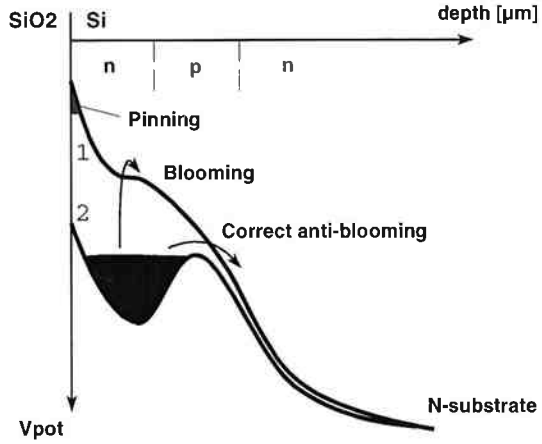

Figure 5: Schematic drawing of potential profiles in vertical cross section (1) under blocking gate and (2) under integrating gate.

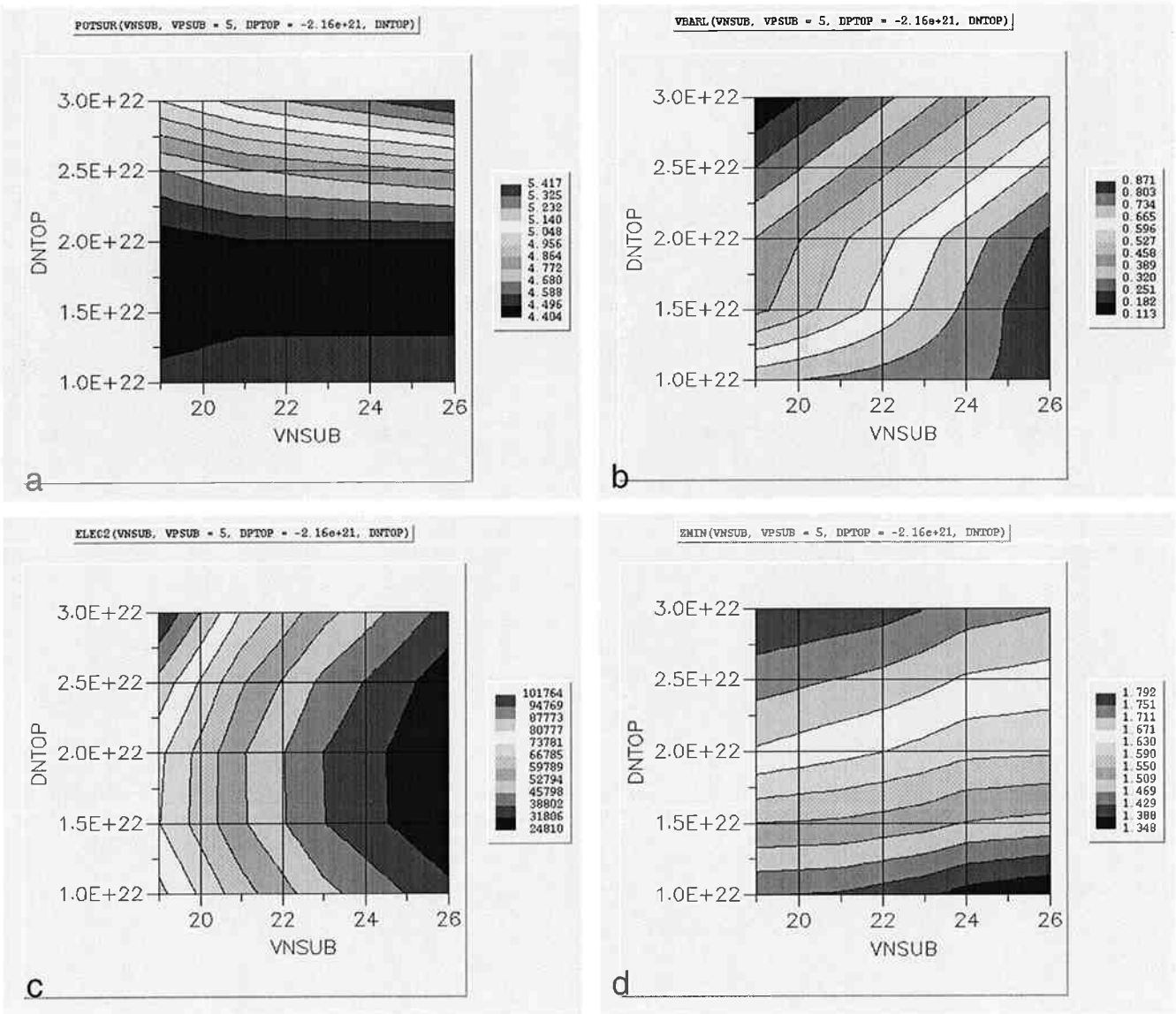

Figure 6: Results of 3D off-state device simulations represented as 2D cross sections of the 4D parameter space: (a) pot_sur, (b) Vbarl, (c) Qmax and (d) z_min as a function of DNTOP and Vns at Vps=5V.