The design of a novel GaAs CCD multiplying D/A converter

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I. Introduction

A MDAC (multiplying D/A converter) refers to a circuit that performs multiplication between an analog signal and a digital word. Since a digital word is in binary form, one common mechanism to implement the MDAC would be to perform successive (binary) divisions on the analog signal; convert the divided signals into currents; and selectively sum them based on the bit values of the digital word. All these steps can be implemented using standard analog/digital circuitries but the amount of circuits involved can be substantial. Normally, in the design of a MDAC, the main concerns are the accuracy and the conversion speed. Our proposed CCD-MDAC consists of a modified CCD structure that performs binary divisions on the analog signal. This produces a sequence of binary-divided charge packets which are proportional to the analog signal. Depending on the bit values of the digital word, these charge packets will be selectively replicated in a second CCD which is synchronized to the original device [1]. As the charge packets move along the second CCD, replicated charges (from the original CCD) are periodically added and the output voltage will be determined by the analog signal and the digital word. As expected, the major advantages of such a MDAC will be its high throughput (to be limited by the clock speed); a reasonably high accuracy (to be limited by the charge transfer inefficiency and precision in defining the areas of the electrodes); and possibly a significant saving in chip area. In many ways, power dissipation in CCDs also compares favorably with shift-registers.

II. Operation of the CCD-MDAC

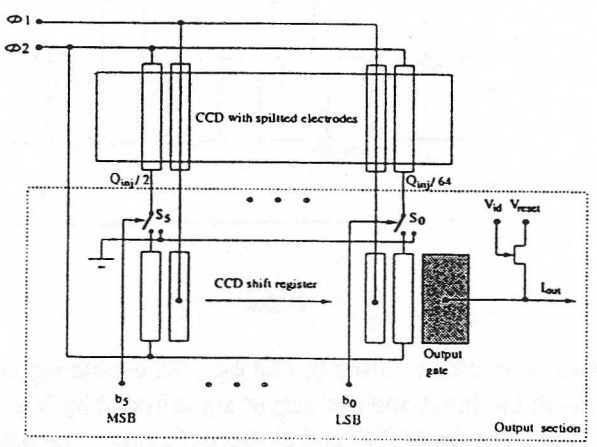

Fig.1

Fig.1 shows the schematic of a proposed CCD-MDAC for 6-bit two-quadrant operation. As observed, the circuit consists of two parts: one part is used in charge divisions and the other part in the multiplication of the analog signals with the digital word. The charge division circuit is a 2-phase CCD with an additional processing step that divides that second electrode in each pixel

into two (equal) halves. This can be implemented by implanting barriers around the lower halves of the second electrodes [2]. As a consequence, only the upper halves of these divided electrodes will take part in charge transfer and every time the analog signal passes through a pixel, the charges will be reduced by a factor of 2. For N pixels, only 2^{-N} of the original charges are transferred to the output. The remaining charges will be held in the lower halves of the divided electrodes. Let us explain briefly how the MDAC would work. Initially, the analog signal is input through the gate G_2 using the fill and spill method and the gate G_1 povides the required dc offset voltage V_r (it can be shown that $V_r = - V_{inmax}$, the maximum value of the input signal if there is to be a 50% full well for zero input). When the clock voltage ϕ_1 is high, charges (i.e., electrons) will flow from the input gate into the first electrode E_1 and will be there temporarily until the clock voltage ϕ_2 turns high (with ϕ_1 going low). The charges then move into the second electrode E_2 but will be divided into two equal halves due to the divided electrodes. This constitutes the first binary division of the signal charges. During the subsequent clock cycles, each time only 1/2 of the charges will be transferred and the remaining charges will be stored in the lower halves of the divided electrodes. The division process is repeated N times for a N-bit MDAC. While the charges are being divided, analog/digital multiplications are also being performed within the same clock cycle. The switch S_5 is controlled by the MSB of the digital word and it determines whether charges in the lower half of the divided electrode are to be replicated in the second CCD. Charge replication can be performed using the wire-transfer technique [3]. Charge transfer is facilitated whenever a "1" exists in the MSB. Otherwise, the stored charges are removed by forward-biasing the electrode momentarily. This same process is repeated for the remaining N - 1 pixels as charges move down the CCDs. The output of the second CCD will therefore be proportional to the product of the analog signal and the digital word.

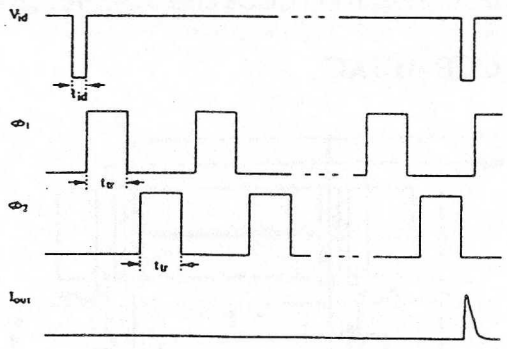

Fig.2

Fig.2 shows the waveforms of clock pulses ϕ_1 and ϕ_2, , the enable signal V_{id}, and the output current. As observed, both the input and the output are initiated by V_{id}. When V_{id} is high, charges will be injected into the first CCD and at the same time, the output is reset to V_{reset}. When V_{id} becomes low, charges are transferred along the CCD until they reach the last pixel, after which V_{id} once again becomes high. During this time, the output current will be sensed using the floating-gate reset sensing technique [4]. As shown in Fig.2, if t_{id} is the time required for input charge injection to occur, this time interval will have to be inserted between ϕ_1 and ϕ_2 to synchronize ϕ_1 and ϕ_2 with V_{id}. For N-bit conversion, the conversion time T_c is therefore given by: $T_c = 2N.(t_{tr} + t_{id})$, where t_{tr} is the transfer time from one electrode to the next.

III. Model simulation

An equivalent circuit for the input and the first CCD-MDAC pixel was used to simulate charge division and multiplication of the MSB. Capacitors are used in the model to mimic the charge storage effect while current sources are used to facilitate charge transport along the CCD. For the purpose of illustration, we assumed an injection current I_{in} as the input. Initially, when ϕ_1, ϕ_2 and V_{id} are all low, the injection current I_{in} will charge up C_o, the capacitance at the input gate G_2, to a value equal to V_o. For a relatively constant I_{in}, $V_o \approx t_{id}.I_n/C_o$. In this work we have included I_d which represents the dark current in the CCD. In practice, $I_d << I_{in}$ and is often ignored.

In the first CCD-MDAC pixel, $C_{1,n-1}$ and $C_{2,n-1}$ represent the capacitances of the first and second electrodes and they are connected to ϕ_1 and ϕ_2. When ϕ_1 is high, $I_{0,n-1}$ charges up $C_{1,n-1}$ and if one assumes that $V_{1,n-1}$ is zero initially, then $V_{1,n-1} = t_{id} \cdot t_{tr} \cdot (1 - \varepsilon).I_{in}/(C_oC_{1,n-1})$, where ε is the charge transfer inefficiency. When ϕ_2 becomes high, charges will flow into $C_{1,n-1}$ and because of the presence of the barrier, only those corresponding to $I_{0,n-1}/2$ will move forward. The balance is stored in lower half of the divided electrodes. In order to reset the storage capacitors, a differentiator circuit consisting of R_d and C_d is added to the equivalent circuit to facilitate discharge at beginning of each clock cycle. The actual simulation of the equivalent circuit was done for a 4-bit CCD-MDAC using SPICE3 as the simulator. The circuit parameters are listed in Table I. For most GaAs CCD, the peak transfer time t_{tr} ranges from between 200-400 ps and a mean value of 300 ps is used here. The injection time t_{id} is estimated to be roughly 50 ps. This would suggest a conversion time of 2.85 ns for a 4-bit CCD-MDAC or a conversion rate of the order of 350 MHz. To facilitate the simulation, we have chosen $t_{id} \cdot t_{tr}/(C_oC_{1,i}) = 1$ for i = 0,1,2....., and n-1 and this sets the voltages across the capacitors $C_{1,i} = (1 - \varepsilon)^i.I_{in}$. All the switches were realized in SPICE3 using a switch model with the fourth terminal grounded. The output voltage of the MDAC was obtained from a 16Ω load. Fig.3 shows a plot of the output voltage when the input was a 0.8 V square wave. As observed, good conversion accuracy has been achieved. The maximum deviation from the ideal outputs was less than 8%.

Circuit parameter	Values
Clock frequency, GHz	1.428
Conversion rate, MHz	357.1
Signal frequency, Mhz	20/25
C_o, pF	50
$C_{1,i}$, $C_{2,i}$, pF	300
R_d, Ω	100
C_d, pF	0.1
V_{to}, mV	250
R_{on}, Ω	10^{-4}

Table I: Parameters used in CCD-MDAC simulation

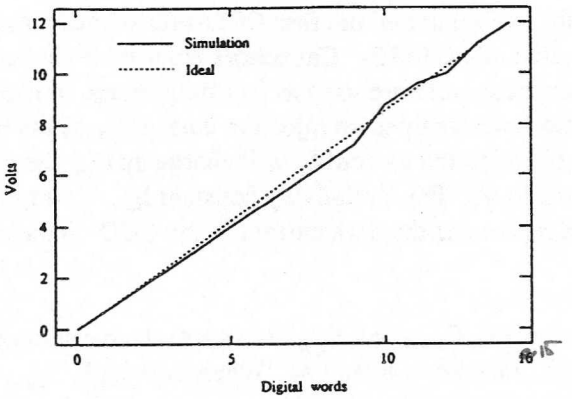

Fig.3

Most MDACs require 4-quadrant operation and this is achieved using the circuit shown in Fig.4. Instead of using the full digital word, the first bit (b_{n-1}) will be made the sign bit. In the figure, two 2-quadrant CCD-MDACs are arranged in parallel. Complementary analog signals are fed to the two CCD-MDACs and a charge subtractor is connected to their outputs to remove the off-set voltage. The charge subtractor could be implemented using the unity gain charge subtractor circuit proposed in [1]. The output of the subtractor will be a current I'_{out} proportional to the analog signal and the digital word except for the sign. To accomodate for this feature, the switch shown in the figure will have to have the following properties: $I_{out} = I'_{out}$ if $b_{n-1} = 1$ and $I_{out} = - I'_{out}$ if $b_{n-1} = 0$.

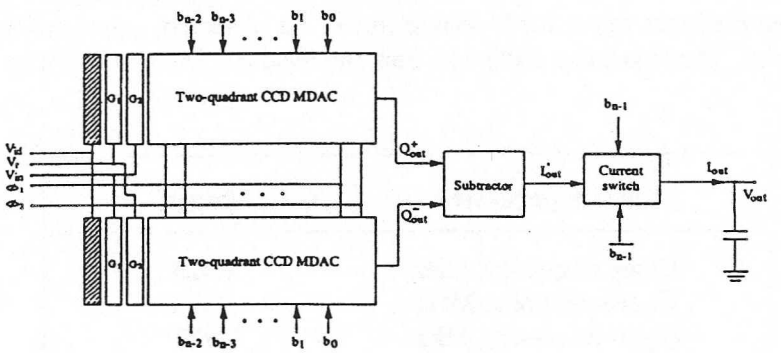

Fig.4

[1] R.E. Colbeth and E.R. Fossum, "A 1 GHz charge-packet replicator/substractor circuit for GaAs CCD signal processing," JIEEE, vol.SC-25, no.4, pp.1016-1019, 1990.
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