A High Resolution, Low Cost CCD Family of Image Sensors for Digital Camera Applications

or "See The Picture Not The Pixels"

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Abstract

Image sensors designed for photographic applications have to be high performance, high resolution and low cost. A family of image sensors designed for this application have 5x10 μm pixels operating with +/- 5V vertical and 0-to-5 V horizontal clocks, 2000:1 dynamic range and 60K e^- well capacity. The sensors also have RGB stripe color filters and sequential color readout multiplexor with resolutions ranging from 700K to 2.5M pixels.

Introduction

Digital still cameras require high resolution high sensitivity, low noise, wide dynamic range and low cost image sensors that will enable them to compete with conventional film cameras. Many of these attributes can be found in today's image sensors that are designed for either video imaging or internet applications. Very few, however, are designed to challenge conventional high quality photography. Sensors that do have photographic quality are often expensive and require system complexity. In this paper we describe the design of a sensor technology that will be used to produce the family of image sensor listed in Table 1. These sensors, are targeted to produce photographic quality images while maintaining low sensor cost, thus enabling simple low cost systems.

Sensor Architecture

A full frame CCD architecture with a 0.8 μm double poly-Si CCD process is utilized to minimize pixel regions without light sensitivity, and to reduce pixel size and chip size without a performance compromise. Figure 1 shows the architecture of the 700K pixel device. The image area of this sensor consists of 5x10 μm^2 pixels organized in 512 lines. The use of 2:1 aspect ratio pixels, shown in Figure 2, results in an image array with two times more resolution in the "x" direction than in the "y" direction. That is, for this specific image sensor with 4:3 aspect ratio and 512 active rows, each line requires at least 1364 pixels to result in square displayed or printed pixels. These 2:1 aspect ratio pixels are designed to be used with RGB stripe color filter array optimized to match pixel spectral characteristics. This architecture enables enhanced color sampling in the horizontal direction while maintaining full color resolution in the vertical direction, while minimizing

color fringes in both directions. The readout section contains a 3:1 multiplexor region, a three-phase horizontal readout register, a high conversion efficiency sense node and a three-stage source follower amplifier. The 3:1 multiplexor separates a line of RGB pixels into three sub-lines, with all of the same color pixels from a given line collected in a sub-line. This readout structure enables gain adjustments in the camera video chain to be optimized for each color. It also simplifies the layout of the horizontal register and increases its well capacity.

Sensor Sub-blocks

The 5 μm wide pixel in Figure 2 is designed for overall system performance. The design criteria include: +/- 5V vertical register clock swing for system simplicity; high well capacity and low noise for a dynamic range of at least 2000:1 to accommodate a large range of photographic scenes; high light sensitivity to result in a camera with ISO speeds comparable to conventional film cameras; antiblooming ratio of at least 500:1; capability to dump image signal into the substrate and clear pixels. To achieve all of these requirements, the poly-Si gates and implants that constitute the pixel have to be well optimized.

In this design a 0.8 μm, minimum design rule, p+ implant, in conjunction with a 2K A° field oxide is used to establish the channel stop sections. The thin LOCOS, increases field threshold considerably with negligible bird's beak extension, and enables the p+ doping to be moderately high, minimizing possibilities for Zener breakdown.

The gate electrode layout maximizes uncovered silicon area to 34% of the pixel area, providing for excellent blue and green light sensitivity. The four-phase two-poly electrode design, when compared to three-poly designs, flattens pixel topology, simplifying wafer processing and considerably increasing yield. The use of minimum design rules, however reduces gate electrode area and increases 3D fringing fields, adversely affecting overall charge storage. Vertical antiblooming in the pixel is achieved through the weak p-well region in the center of the pixel established by an opening in the p-well pattern. Figure 3 shows a cross-section of a half pixel highlighting the buried channel, p-well and substrate junctions. The signal charge is stored in the n-buried channel region and extra charge drains towards the substrate. The buried channel and the p-well doping profiles are selected through an optimization routine that maximizes electrode well capacity and accounts for blooming margin to the off gate, surface channel margin to the SiO_2 interface and antiblooming threshold to the substrate. Figure 4 is an example of an optimization chart that shows the contours for well capacity as well as the limits to blooming, injection, pinning and surface channel. This pixel design with +/- 5V gate electrode biases maintains good antiblooming properties of 500X while achieving a high well capacity of 60K electrons.

Figure 5 shows pixel signal and noise, in electrons, as a function of light intensity. The dynamic range of the pixel is about 6000:1, which is well above the required level. For a dark noise of 10 e^- and response FPN of 0.5% the SNR is dominated by dark noise at low

illumination and by signal shot noise at mid-light and high-light levels. Only at saturation the response FPN becomes significant.

With the same system considerations in mind, the horizontal register is designed out of two layers of poly-Si as a three-phase CCD, operating at 0-to-5 V clock swings, that can easily be provided by inexpensive CMOS line drivers in the camera system. The multiplexor uses a combination of vertical clocks and horizontal clocks to achieve the 3:1 pixel separation. This architecture eliminates the use of additional transfer clocks or multiplexor clocks, further simplifying system requirements.

The sense node and output buffer are designed for low noise and high speed operation. As shown in Figure 6, the last CCD gate surrounds the sense node, with the large charge storage area closely spaced for fast charge transfer. The p-well is depleted on all sides of the sense node to minimize capacitance and clock noise coupling. The total effective capacitance of the sense node is about 7 fF, giving 22 μv/e$^-$ at the input of the buffer. The first transistor of the buffer is located adjacent to the sense node, to minimize capacitance. At the normal operating voltages, the p-well under its channel is fully depleted, reducing body effects and increasing gain.

The buffer consists of three stages, all surface channel, giving an overall gain of 0.6 with a bandwidth in excess of 150 MHz.

Results and Conclusions

This architecture has been implemented in the 1/2 in format with 700K pixels. Early results show that almost all of the design targets have been achieved. The vertical clocks operating with +/-5V rails result in typical saturation signals of 750 mV. The device was operated with good performance at pixel rates of up to 50 MHz, without degradation in horizontal register CTE. The first stage dominates the buffer's noise, with a noise spectral density of 8 nv/rt-Hz, or 100 μV RMS noise in a 40 MHz bandwidth after CDS, referred to the CCD output. With these performance parameters, implementation of the two other sensors with larger pixel counts is easily achievable.

Resolution	format	Horizontal pixels	Vertical Pixels	Diagonal
700K	1/2"	1380	512	8.5mm
1.6M	2/3"	2062	768	12.8mm
2.5M	1"	2574	960	16mm

TABLE 1. Targeted Image Sensors

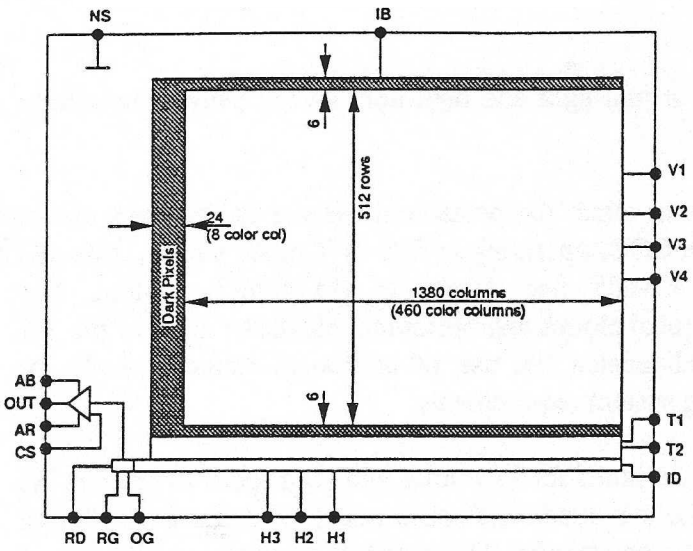

Figure 1. Sensor Architecture

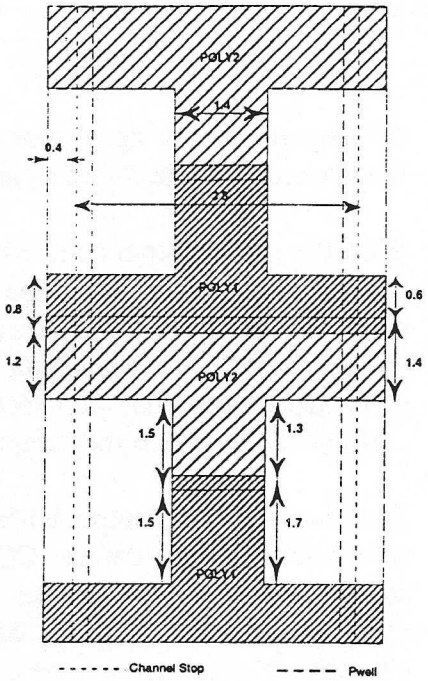

Figure 2. Pixel Layout

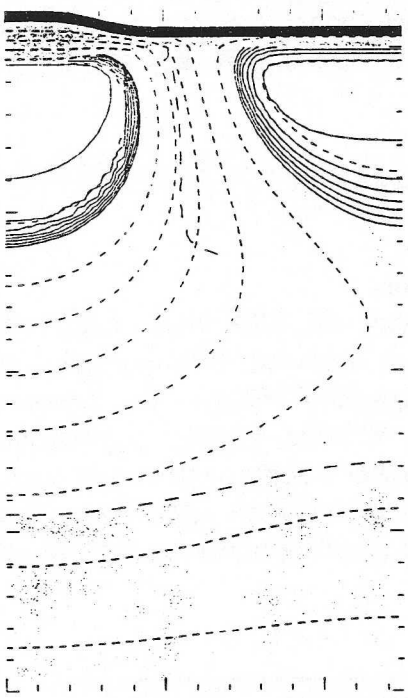

Figure 3. Pixel Structure and Potential Profiles

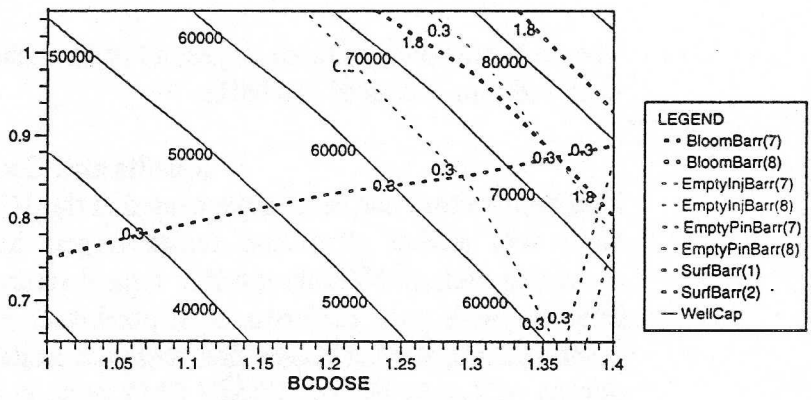

Figure 4. Doping Optimization Chart

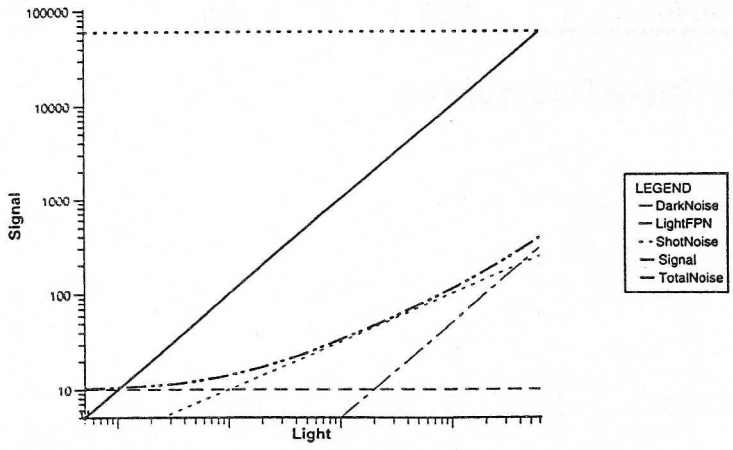

Figure 5. Sensor SNR vs Illumination

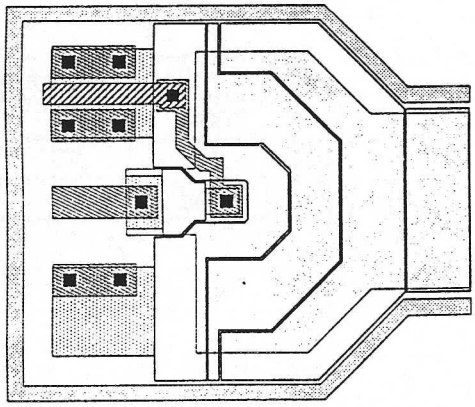

Figure 6. Sense Node Layout

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