# Active Pixel Image Sensors in 0.35μm CMOS Technology

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We have successfully designed, fabricated and tested a group of CMOS active pixel sensor (APS) chips in a 0.35um ASIC CMOS process. Images with 70 dB dynamic range were captured with a supply voltage of 3.3V.

CMOS imaging has received considerable attention in the last few years as a viable imaging technology[1]. CMOS sensors with image quality comparable to CCDs have been demonstrated by several groups[2 3 4]. Scaling of CMOS technology can have both positive effects (pixel size, power, cross talk) and negative effects (noise, quantum efficiency, dynamic range) on the CMOS APS[5].

Our design is based on the JPL architecture[2] with modifications in the control circuitry for added functionality. The image sensor consists of an array of pixels, row and column decoders, clock generators and readout circuitry (Figure 1). The readout circuit consists of a source follower and reset transistor within the pixel and two sample and hold circuits in the column (Figure 2). Both photodiode and photogate type sensors are studied. Normal operation of the sensors is in scanning mode as described in the above reference. Correlated-double-sampling is used to suppress 1/f noise, kTC noise and fixed pattern noise in the pixels. The photogate designs can also be operated in snapshot mode at the cost of true CDS readout.

The designs were implemented as 512 × 384 pixel test chips in a 3.3 V 0.35 μm ASIC CMOS technology. This process offers smaller pixel size, higher conversion gain, lower power operation and higher speed than older technologies. The only deviation from the standard single-poly 4-metal process is the use of a silicide block over the sensing region. The metal-4 layer is not used for routing and is used as a light shield on some wafers. The pixel size is 8μm x 8μm with fill factors varying from 25% and 35%. The chip size is 5.9 × 4.7 $mm^2$.

The image sensors are operated with a 3.3V power supply and two additional d.c. voltages. Image quality is comparable to previously reported CMOS sensors with typical saturation levels of 1.2V and dynamic range of 70 dB for the photodiode sensor (Figure 3). Conversion gain at 9.5 μV/$e^-$ and 42 μV/$e^-$ for the photodiode and photogate designs respectively, is significantly higher due to lower output node capacitance. The photodiode pixel dark current is an order of magnitude lower than in the photogate pixel. Quantum efficiency is

generally lower peaking at 20% in the photodiode sensor and 14% in the photogate sensor. Spectral response is flatter than in older technologies possibly due to shallower junction depth and epi thickness in this process. Raw fixed pattern noise is between 6-8% of saturation and can be reduced to less than 1% using the crowbar circuit. Additional improvements would require frame subtraction or gain correction as well. Power dissipation is approximately 25 mW at 30 Hz frame rate operation. The sensors are functional with a supply voltage as low as 1.8V. Although the photodiode saturation level decreases to 300 mV and fixed pattern noise becomes more apparent the dynamic range is approximately 54 dB . These results are summarized in Table 1.

Of the four pixel designs studied, the regular photodiode sensor yielded the best performance with higher dynamic range and lower dark current than the photogate designs. The photodiode with a transfer gate had higher responsivity but also showed higher lag. The regular photogate design had high dark current and low quantum efficiency resulting in poor responsivity. The square photogate with smaller gate area showed better performance due to higher light transmission through the open regions and lower dark current. Since saturation is limited by the output circuitry and not the well capacity, shrinking the gate area is suitable for applications that require a photogate pixel.

The authors would like to thank Horng-Sen Fu, Mike Cox, Victor Wang and the ULSI Research Fab personnel for device fabrication, ULSI Lab technical staff and management for supporting the CMOS APS research project and Khoa Tran and Gary Gordon of ICBD for helping with chip layout.

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[1] E. Fossum "Active Pixel Sensors -- Are CCDs Dinosaurs?" *Proceedings of the SPIE,* vol. 1900, 1993.
[2] S. Mendis et al, "CMOS Active Pixel Image Sensor" *Transaction on Electron Devices,* vol. 41(3), 1994.
[3] A. Dickinson et al, "A 256x256 CMOS Active Pixel Image Sensor with Motion Detection," *IEEE ISSCC Technical Digest,* 1995.
[4] P. Denyer et al, "CMOS Image Sensor for Multimedia Applications," *IEEE Proc. CICC,* 1993.
[5] P. Wong, "Technology and Device Scaling Considerations for CMOS Imagers," *Transactions on Electron Devices,* vol. 43(12), 1996.

**Figure 1: CMOS APS Chip Architecture**

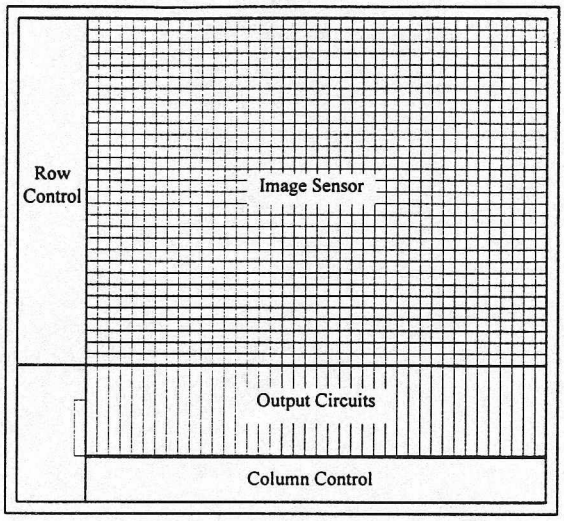


**Figure 2: Schematic of Pixel and Readout Circuitry**

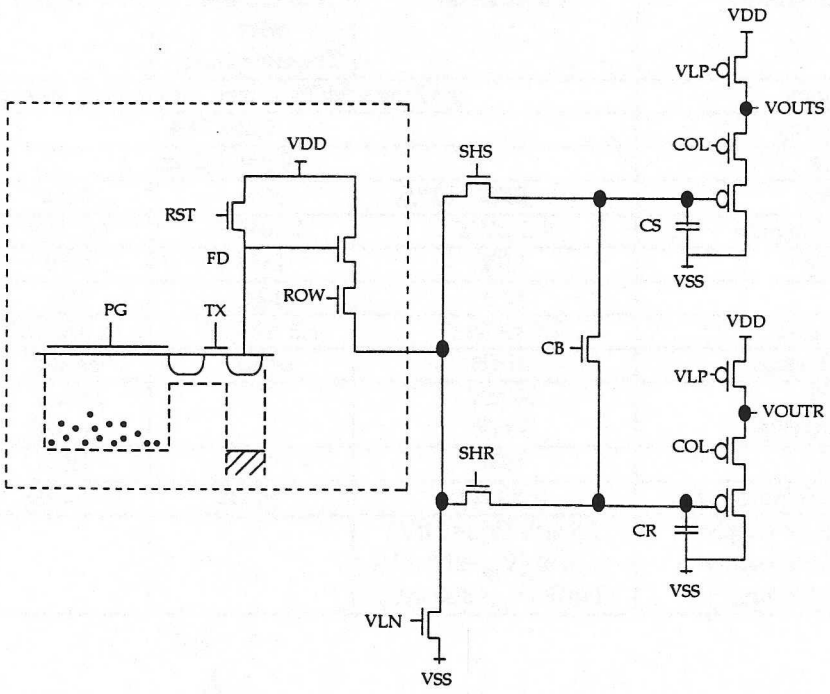

**Figure 3: Image from Test Chip with Photodiode Pixels**

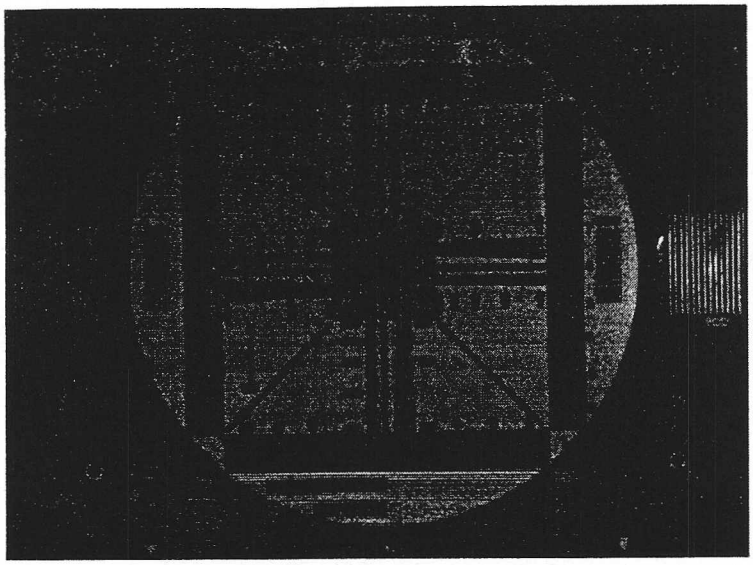

**Table 1: Summary of Results**

| Pixel design | Photodiode | Photodiode with Transfer Gate | Photogate | Square Photogate |
|---|---|---|---|---|
| Technology | 0.35 μm CMOS, n-well, single-poly, 4-metal | | | |
| Imager array | 512 × 384 | | | |
| Pixel size | 8 μm × 8 μm | | | |
| Fill-factor | ~~35%~~ 43% | 30% | 25% | 25% |
| Conversion gain | 9.5 μV/$e^-$ | 54 μV/$e^-$ | 42 μV/$e^-$ | 43 μV/$e^-$ |
| Saturation | 1.2V | 1.0V | 1.0V | 1.0V |
| Noise | 42 $e^-$ | 12$e^-$ | 15$e^-$ | 13$e^-$ |
| Dark current | 2.6 nA/$cm^2$ | 1.2 nA/$cm^2$ | 11 nA/$cm^2$ | 3.5 nA/$cm^2$ |
| Dynamic range | 70 dB | 64 dB | 64 dB | 65 dB |
| Raw FPN<br>Corrected FPN | 74 mV<br>3 mV | | 86 mV<br>10 mV | |
| Peak QE | 19% | | 12% | |
| Maximum Frame rate | > 50 Hz | > 50 Hz | > 50 Hz | > 50 Hz |
| Power: 3.3V supply<br>2.5V supply<br>1.8V supply | 25 mW ($V_{sat}$=1.0V)<br>12 mW ($V_{sat}$=600 mV)<br>2 mW ($V_{sat}$=300 mV) | | | |