A Low Smear p-substrate Frame Interline Transfer Sensor with kTC Noise Reduction

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1. Introduction

An interline transfer image sensor was developed for an application demanding low image smear and low dark current. A -100dB image smear was required to avoid visual artifacts at short (1ms) exposure times. A 0.1nA/cm^2 dark current (T=25°C) was required to maintain good S/N when imaging at 65°C. Other sensor requirements were 11.5µm(H) x 13.5µm(V) pixels, good responsivity across the visible spectrum, 100x antiblooming, and an 80µs exposure control.

The image sensor was fabricated on a p-substrate with a 1.5µm, 1X stepper technology. Generally, p-substrate sensors are not suitable for low smear applications due to excessive carrier crosstalk. However, we have developed a PTUB technology to achieve a 20x crosstalk reduction.

2. Architecture and Operation

The sensor architecture, illustrated in Figure 1, is called a Fast Frame Interline Transfer (FFIT) architecture. All control signal are metal-strapped to allow very fast clocking of the image, isolation and storage regions including exposure control. The image region has 768(H) x 498(V) pixels arranged in an interline format. The pixel (Figure 2) consists of a pinned-photodiode, an antiblooming / exposure control structure, and a VCCD. The 8-row isolation region minimizes crosstalk into the storage region. An independent lateral drain removes excess smear charge.

The 250 row storage region holds an entire field of image data during readout. Low dark current is achieved by employing thin oxide channel stops and by biasing all gates into pinning during line readout. Signal capacity is maintained by storing charge under all four gates; the first half of the CS1 electrode is boron-implanted to create a barrier. Signal capacity is maintained by storing under all four gates. A unique feature of the storage region is the lateral drain (Figure 4) which allows a near instantaneous flushing of dark signal prior to frame transfer.

A field readout contains six clocking intervals: an optional exposure control pulse, a dump of the storage region into its lateral drain, a clearing of the image region VCCD into the isolation region drain, a pixel-to-VCCD transfer, an image-to-storage VCCD transfer, and a readout of the storage region. The metal-strapping allows very fast transfer times. Vertical clocks typically operate at 3.5MHz. Horizontal readout is at 14MHz. A very short (<1µs) exposure times are possible although frame transfer smear increases at short exposure times.

3. Smear Reduction Techniques

Commercial ILT image sensors now achieve -80dB to -100dB image smear. These sensors combine very low reflectivity tungsten metalization, sub-micron design rules, and vertical antiblooming. We had previously constructed an experimental ILT sensor with standard p-substrate CCD processing and measured -30dB image smear. To exceed the -100dB with a p-substrate and 1.5µm design rules, we developed a low crosstalk CCD process and a low smear CCD architecture.

Image smear in p-substrate image sensors is dominated by carrier diffusion: a large fraction of photogenerated electrons are created deep in the silicon below the image pixel electric fields and some diffuse laterally into the adjacent vertical CCD. We developed the antismear PTUB technology to minimize this electron diffusion into the VCCD. As illustrated in Figure 2, the VCCD channel is contained within a boron implanted PTUB. The doping distribution is illustrated

in Figure 3. The PTUB doping concentration N_{A2} is greater than the substrate doping concentration N_A creating a potential barrier equal to $(kT/q)\ ln(N_{A2}/N_A)$. For $N_{A2} = (10)^{16}cm^{-3}$, $N_A = 5(10)^{14}\ cm^{-3}$, this barrier blocks approximately 90% of the photogenerated electrons, translating to a 20dB smear improvement over conventional p-substrate sensors. The PTUB also reduces the VCCD depletion depth which provides an estimated 6dB additional smear improvement.

Image smearing only occurs during the image VCCD transfer interval. The FFIT architecture significantly reduces this time to 72µs compared to 16ms for an ILT device lacking a storage region. This represents a 47dB smear improvement. Although pixel-to-VCCD crosstalk outside of the VCCD transfer interval does not contribute to smear, it can accumulate and possibly overflow the VCCD structure. The lateral drain in the isolation addresses this issue by allowing charge in the image VCCD to drain away during the integration period.

We modeled the pixel-to-VCCD crosstalk using Luminous in the Silvaco simulator. It predicted a carrier crosstalk of 0.5% at 630nm and 1.7% at 900nm. Simulations of a non-PTUB device predicted 9.6% crosstalk at 630nm and 35.6% crosstalk at 900nm. The measured crosstalk for a PTUB device was 2.1% at 670nm and 1.1% at 900nm. Light piping may be responsible for the higher crosstalk at 670nm. The 2.1% crosstalk translates to a -100dB image smear.

4. Noise Reduction

The sensor has a floating gate output node (Figure 5). Adding and removing signal electrons from a floating gate node are essentially noiseless operations. *kTC* noise is only introduced during the floating gate reset. By resetting this gate once at the start of the line, the *kTC* noise can be determined before signal is read out. We sample the *kTC* noise on the initial 6 dark pixels. This technique only requires 1/2 the bandwidth and sampling speed of conventional methods.

Measurements confirm that *kTC* noise (calculated to be 70e^-) has been eliminated. The RMS noise on the video was measured at less than 40 electrons and was probably dominated by system noise. No degradation by *1/f* noise was observed.

5. Measurements

The sensor has been fabricated and characterized. It produced good imagery and the performance characteristics are summarized in Table I. This sensor provides good responsivity throughout the visible and into the NIR as illustrated in Figure 6.

Table I - Performance characteristics

Parameter	Value
Image Smear	-100 dB (V/10 method)
Dark Current (25C)	0.1 nA/cm^2 at 25°C
Random Noise	< 40 e^-
Signal Capacity	60,000 e^-
Fill Factor	25%
Blooming Suppression	> 100x (10% spot size blooming to 20%)
Charge Conversion Efficiency	3 µ*V*/e^-

6. Conclusions

We have demonstrated a p-substrate image sensor with excellent image smear and low dark current suitable for both visible and NIR imaging. The FFIT architecture allows for very high speed image clocking and exposure control. The output structure allows a simplified *kTC* subtraction circuit.

FIGURE 1 - FFIT ARCHITECTURAL DIAGRAM

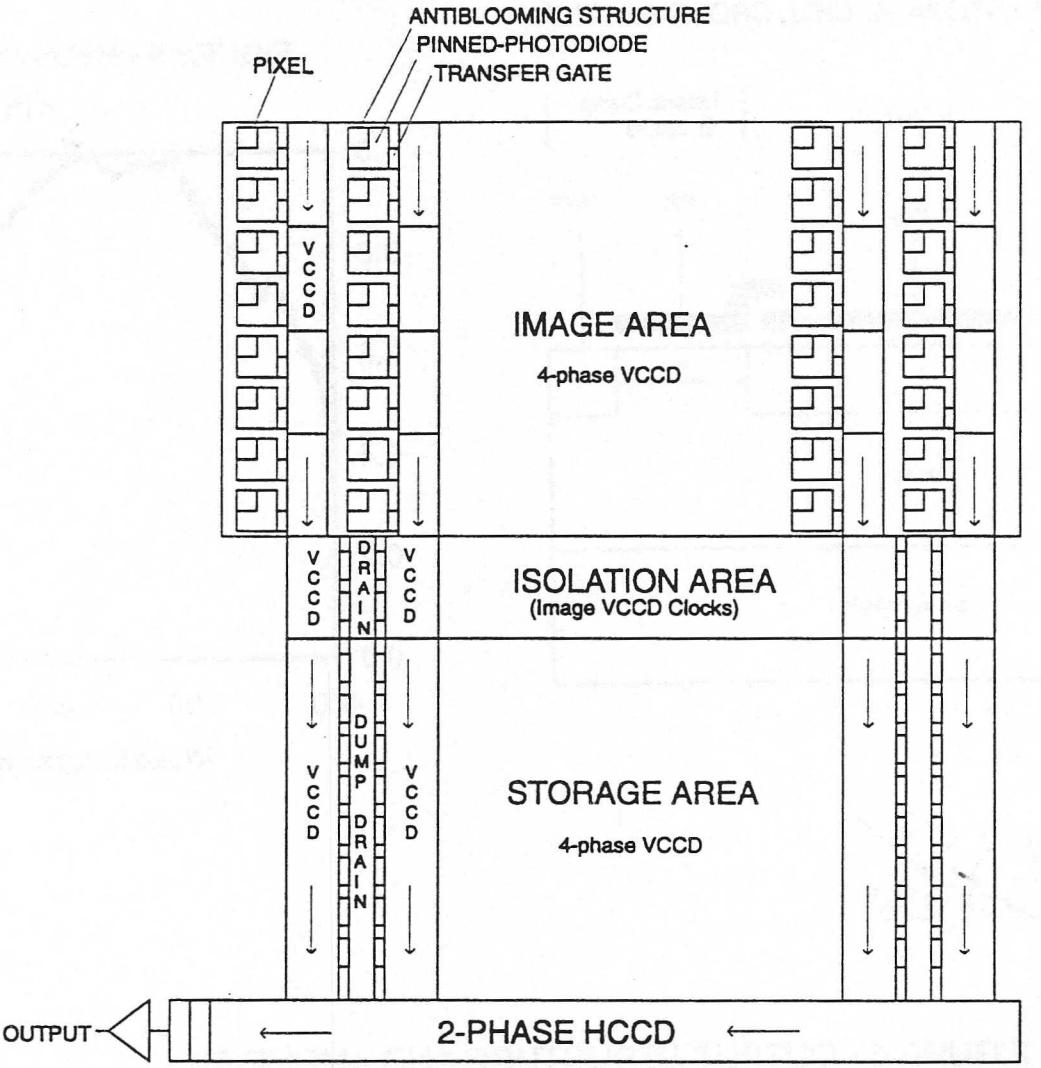

FIGURE 2 - IMAGE CELL CROSS SECTION

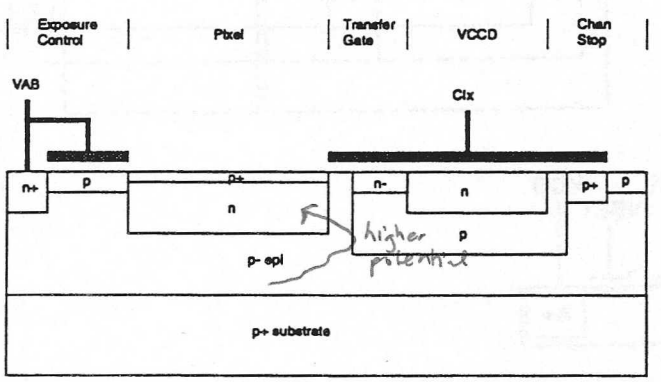

FIGURE 3 - PTUB DOPING PROFILE

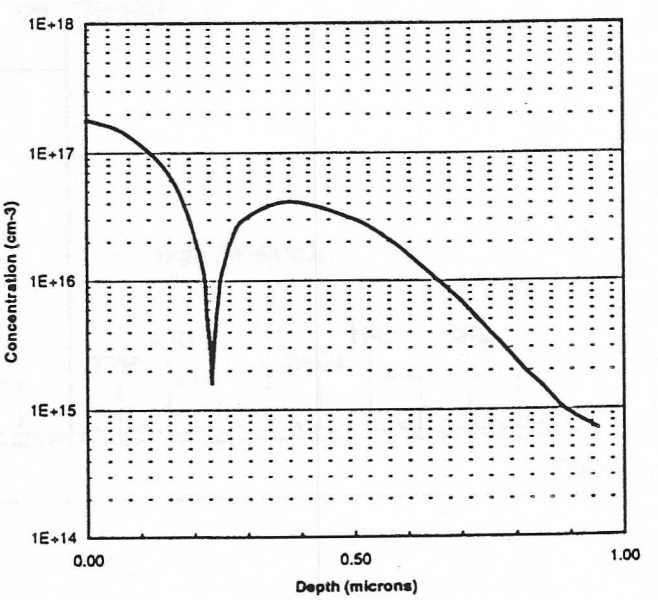

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FIGURE 4 - STORAGE CELL CROSS SECTION

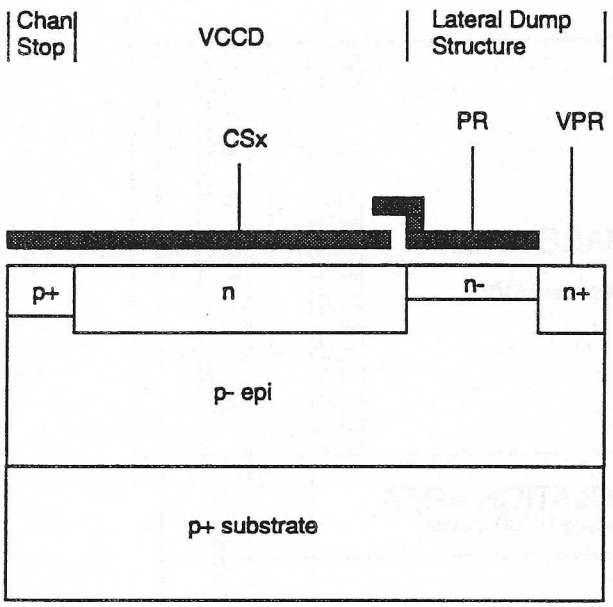

FIGURE 6 - Relative Responsivity

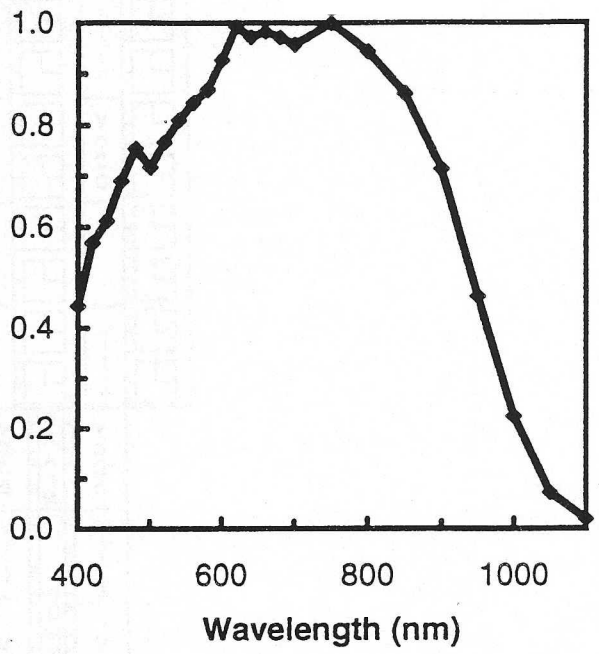

FIGURE 5 - OUTPUT STRUCTURE AND AMPLIFIER