Driving Voltage Reduction of Shift Registers in IT-CCD Image Sensors

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Abstract- **We have clarified limitations to driving voltage reduction in both vertical and horizontal registers in IT-CCD image sensors. For vertical registers, which consist of 3 or 4 phase CCDs, decrease in charge handling capacity due to thermionic emission determines the limit and the driving voltage cannot be reduced less than 0.8 ~ 0.9 V in a typical case. For horizontal registers, which consist of 2 phase CCDs, charge transfer degradation due to potential pockets under the inter-electrode gaps determines the limit and the driving voltage appears to be reducible to 1.1 V.**

I. Introduction

In order to reduce power consumption in CCD image sensors, driving voltages of both vertical and horizontal shift registers strongly need to be reduced. Generally, in interline-transfer CCD (IT-CCD) image sensors, 3 or 4 phase CCDs operated typically with 5 ~ 9 V amplitude transfer pulses are applied to vertical registers, while 2 phase CCDs operated typically with 3 ~ 5 V amplitude transfer pulses are applied to horizontal registers. In this paper we report analyses concerning driving voltage reduction and its limitations for vertical CCD registers (V-CCDs) and horizontal CCD registers (H-CCDs).

II. V-CCD Driving Voltage Reduction

An important factor that should be paid attention to when reducing V-CCD driving voltage is decrease in charge handling capacity due to thermionic emission[1],[2]. Because electrons have thermal energy, in order to store electrons in a well, a potential barrier height (the difference in potential between an electron storing well and its surrounding barrier region) must be sufficient to keep them from overflowing.

We have based our analysis of barrier height upon the model shown in Fig. 1 and the following assumptions: 1) The time required for single-stage charge transfer is much shorter than the periods between transfers; 2) charge transfer is complete, i.e. there is no loss of charge during the transfer; and 3) all wells through which charge is transferred have the same structure. In this sense, it is as if a charge were being held in a single well during the time t_{FS} that is required for full-stage charge transfers throughout a CCD register. (For V-CCDs in a NTSC mode, t_{FS} is 1/60 sec.)

The overflow current I may be expressed as a function of barrier height V_B:

$$I = I_0 \exp\left(-\frac{q}{kT}V_B\right), \qquad (1)$$

$$I = -\frac{dQ}{dt} = C\frac{dV_B}{dt}, \qquad (2)$$

where I_0 is a current coefficient, which is a function of the semiconductor device's structure and its impurity concentration, Q is the stored charge quantity, and C is the capacitance of the well. Solving (1) and (2) with the initial condition that $V_B=0$ at time $t=0$ and substituting $t=t_{FS}$, we can get an equation that describes the barrier height dependence on t_{FS}:

$$V_B = \frac{kT}{q}\log\left(\frac{qI_0 t_{FS}}{kTC}+1\right). \qquad (3)$$

To determine the magnitude of the barrier height V_B for a typical V-CCD structure, values for I_0 and C need to be obtained. For this purpose, we conducted computer simulations, where we varied discretely the quasi-Fermi level in the electron storing well and examined the V_B dependence of overflow current I and stored charge quantity Q. I_0 is then given by V_B dependence of I using (1) and C is given by $\Delta Q/\Delta V_B$.

We consider structural parameters, such as the N-layer width W, (barrier-)electrode length L and N-layer impurity concentration N_D, which may affect the barrier height. Although W affects I_0 and C, it does not affect V_B. This is because both I_0 and C increase linearly with increases in W, and as (3) shows, the two effects cancel each other out. As shown in Fig. 2, the barrier height V_B decreases from 0.55 V to 0.47 V as the electrode length L increases from 3 μm to 9 μm. As shown in Fig. 3, the barrier height V_B ranges from 0.51 V to 0.55 V according to the impurity concentration N_D differences ranging from $6\times10^{+16}$ cm^{-3} to

$3\times 10^{+16}$ cm^{-3}.

It is noted that the barrier height V_B does not depend greatly on the structural parameters, and the V_B value is within the range between 0.5 V and 0.55 V for typical cases. This corresponds to the gate voltage difference of about 0.8 ~ 0.9 V, because the ratio of channel potential variation to the gate voltage in buried channel CCDs is about 0.6. This result means that with less than about 0.8 ~ 0.9 V amplitude transfer pulse V-CCDs cannot transfer any charges. This determines the limitation of the driving voltage reduction of V-CCDs.

We measured the charge handling capacity of 4-phase V-CCDs in a 1/4-inch 250K-pixel IT-CCD image sensor while lowering the transfer pulse amplitude (raising low level voltage of the transfer pulse). The results obtained are shown in Fig. 4. It was found that the charge handling capacity decreased linearly with decreasing amplitude and became 0 at an amplitude of 0.9 V. This value agrees well with our simulation result.

III. H-CCD Driving Voltage Reduction

A main factor that limits driving voltage reduction in H-CCDs is degradation of charge transfer efficiency due to potential pockets, which may be induced under the inter-electrode gaps[3],[4] by reducing the driving voltage.

We simulated channel potential profiles for a 2 phase CCD, whose barriers are formed by boron ion-implantation, to search for a method for suppression of the pockets. Our simulation results indicate that aligning the edge position of the potential barrier region X_b, defined as the mask edge position, with that of the storage electrode effectively suppress the pockets[5].

Figs. 5 (a) and (b) show, respectively, simulated channel potential profiles at various boron doses and at a driving voltage of 3 V for two separate conditions: Condition I, in which the edge position X_b was aligned with that of the barrier electrode; and Condition II, in which it was aligned with that of the storage electrode (optimum barrier region alignment). The parameters of the simulated CCD structure were as follows. Peak concentrations for the n-well and the p-well were $8\text{x}10^{16}$ cm^{-3} and $2.5\text{x}10^{15}$ cm^{-3}, respectively, and the p-n junction was about 0.6 μm below the substrate surface. The inter-electrode gap length was 0.2 μm, the length per transfer stage was 10 μm, and gate-oxide and electrode thicknesses were 0.07 μm and 0.3 μm, respectively. Both graphs indicate that a small boron dose induces a potential pocket A, while a large boron dose induces a potential pocket or bump B. Potential pockets/bumps are less likely to be generated in Condition II.

Figs. 6(a) and (b) show boron doses at which potential pockets/bumps just begin to be generated with respect to driving voltage in Condition I and II, respectively. In Condition I, a driving voltage less than 2.6 V induces potential pockets/bumps at all boron doses, which means the minimum driving voltage for which it might be possible for no potential pockets/bumps to be generated would be 2.6 V (at a dose of $4.5\text{x}10^{11}$ cm^{-2}). In Condition II, region 1 is larger than that in Condition I, and the minimum driving voltage appears to be reducible to 1.1 V (at a dose of $2.5\text{x}10^{11}$ cm^{-2}).

IV. Summary

We have analyzed factors which limit driving voltage reduction in both V-CCDs and H-CCDs in IT-CCD image sensors.

For V-CCDs, decrease in charge handling capacity due to thermionic emission determines the limit. On the basis of thermionic emission, we have clarified that the barrier height is about 0.5 ~ 0.55 V for typical cases. This corresponds to the gate voltage difference of about 0.8 ~ 0.9 V, which determines the limitation of the driving voltage reduction of V-CCDs.

For H-CCDs, on the other hand, charge transfer degradation due to potential pockets under the inter-electrode gaps determines the limit. Our simulation results indicate that aligning the edge position of the potential barrier region with that of the storage electrode effectively suppress the pockets. At an optimum boron ion-implantation into the barrier region, minimum driving voltage appears to be reducible to 1.1 V.

References

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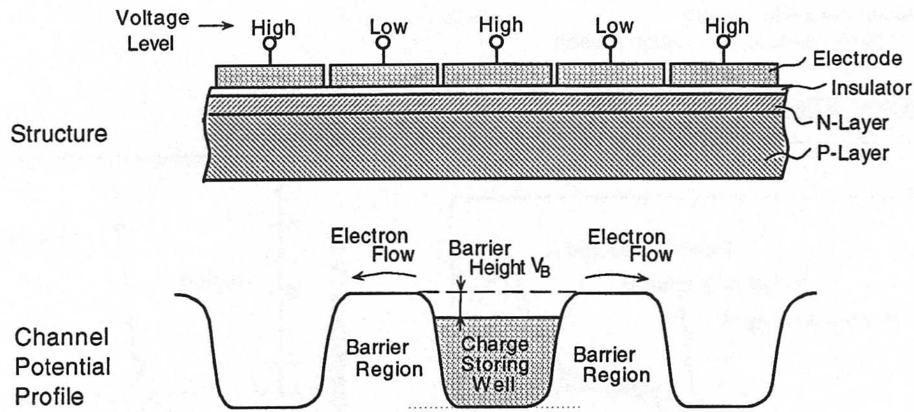


Fig. 1 The structure of CCD register with its channel potential profile upon which our thermionic emission analysis is based. Potential well under the center electrode is filled with electrons. Storing electrons in a well requires a sufficient potential barrier to keep them overflowing.

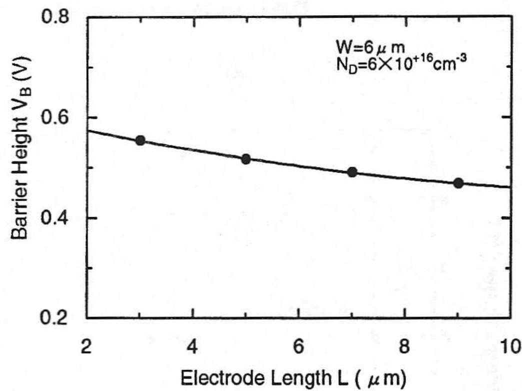


Fig. 2 Barrier height value V_B as a function of electrode length L obtained from simulation results, where channel width W is 6 μm and N-layer impurity concentration N_D is 6×10^{16} cm^{-3}. The barrier height is from 0.55 V to 0.47 V according to the variation in electrode length from 3 to 9 μm.

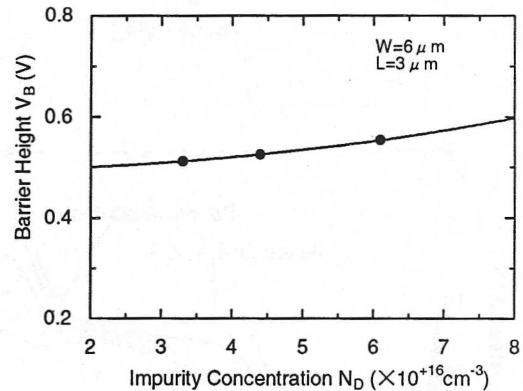


Fig. 3 Barrier height value V_B as a function of N-layer impurity concentration N_D, where channel width W is 6 μm and channel length L is 3 μm. The barrier height is from 0.51 V to 0.55 V according to the variation in N-layer impurity concentration N_D from 6×10^{16} cm^{-3} to 3×10^{16} cm^{-3}.

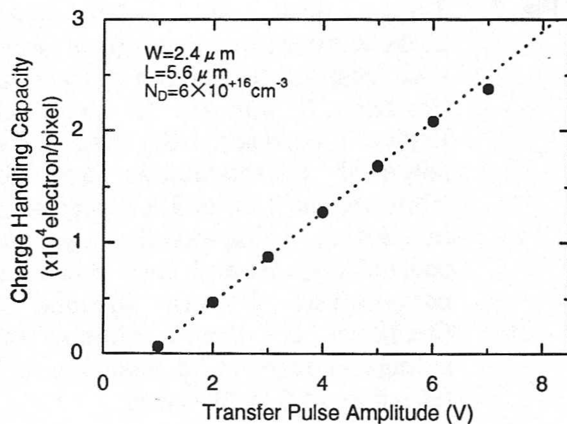
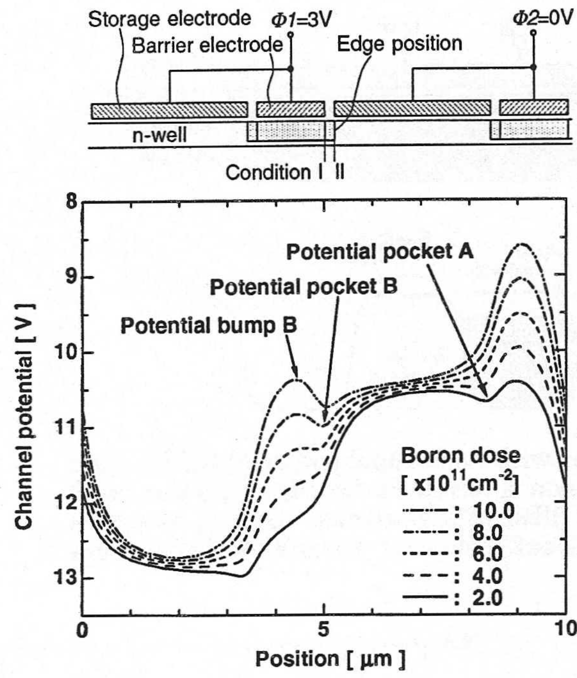
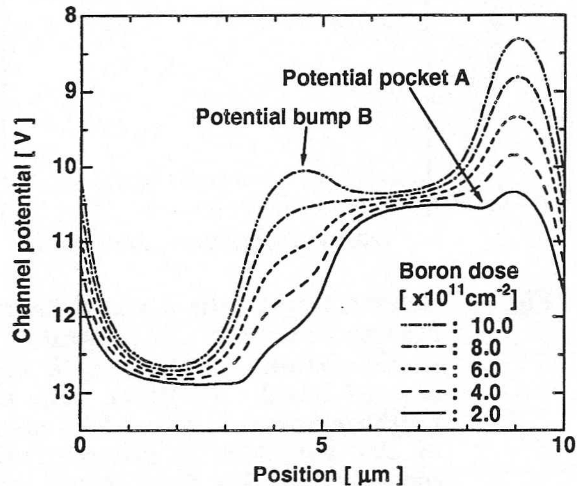


Fig. 4. Measured dependence of charge handling capacity on transfer pulse amplitude in a 1/4-inch 250K-pixel IT-CCD image sensor. Channel width W is 6 μm, electrode length L is 5.6 μm, and N-layer impurity concentration N_D is 6×10^{16} cm^{-3}. To be exact, L is defined as the length of the total "off-state" electrode region (adjacent two electrode region). Charge handling capacity decreases linearly with decrease in the transfer pulse amplitude and it becomes zero when the amplitude is about 0.9 V

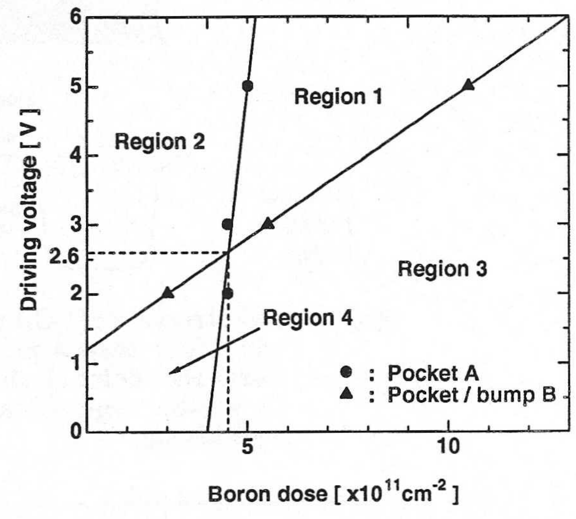


(a)

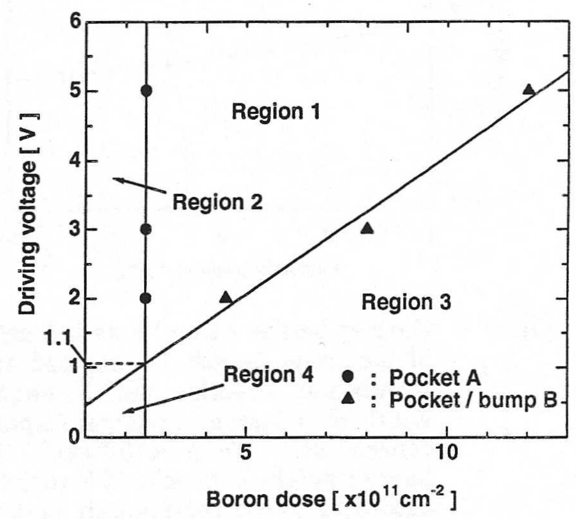


(b)

Fig. 4 Simulated channel potential profiles at various boron doses (a) in Condition I (aligning the edge position of the potential barrier region with that of the barrier electrode, Xb=0) and (b) in Condition II (aligning the position with that of the storage electrode, Xb=0.2 µm). A small boron dose induces a potential pocket A, while a large boron dose induces a potential pocket or bump B. Potential pockets/bumps are less likely to be generated in Condition II.



(a)



(b)

Fig. 5. Boron dose at which potential pockets/bumps just begin to be generated with respect to driving voltage (a) in Condition I and (b) in Condition II. Region 1 represents the areas in which potential pockets/bumps are absent, while region 2, 3, and 4 represent areas in which, respectively, pocket A, pocket/bump B, and both pocket A and pocket/bump B are present. In Condition II, the minimum driving voltage appears to be reducible to 1.1 V (at a dose of 2.5×10^{11} cm^{-2}).