Offset-free offset correction for active pixel sensors

Bart DIERICKX Guy MEYNANTS Danny SCHEFFER
IMEC, Kapeldreef 75, B-3001 Leuven, Belgium • dierickx@imec.be

1. Introduction

The output signal of active pixels has a non-uniformity caused by technological variations of the electronic components composing the pixel. If no precautions are taken, this non-uniformity (fixed pattern noise or FPN) is seen as a "snow-like" shade over the image.

We describe a method to improve the reading of active pixels, so that this FPN is cancelled, with as final result a better *cosmetic quality* of the image. Several solutions to this problem have been proposed in literature. We described a technique based upon shifting the threshold voltage of the source follower transistor in the pixel [1] and a correction technique with a dedicated co-processor [2]. The solution proposed here is a correlated double sampling technique, which is a widespread technique to tackle this problem for integrating pixels [3, 4, 5].

For this purpose, it must be possible to bring the active pixels in a reference state that corresponds to a known amount of collected light. In integrating pixels, the state corresponding to "dark" can be used as "reference state" or "reset state" of the pixel, as it is available after the pixel reset. The correlated double sampling operation subtracts the output signal of each pixel from its reference state. This operation is done in column amplifiers, placed at the edge of the pixel matrix. The difference is obviously free of the pixel's offset non-uniformities. However, if the column amplifiers are composed of *imperfect* electronic component themselves, a new column-wise non-uniformity will result. The circuit proposed here tackles also its own sources of non-uniformity.

2. Offset compensating column amplifier

We propose a circuit that executes the subtraction of the reset-level from the signal level, and that moreover does not introduce any new non-uniformity. Fig. 1 shows a simple 3-transistor active pixel. Its principle is clear. After a fixed integration time, the optically generated charges are accumulated on the junction capacitance of the photo diode. At readout, the selection transistor is closed and the pixel's source follower puts the diode voltage on the column bus. A reset pulse drains the accumulated charges and forces the pixel in its "reference state". Sources of non-uniformity in the pixel are the threshold voltage variation of the source follower and the reset transistor.

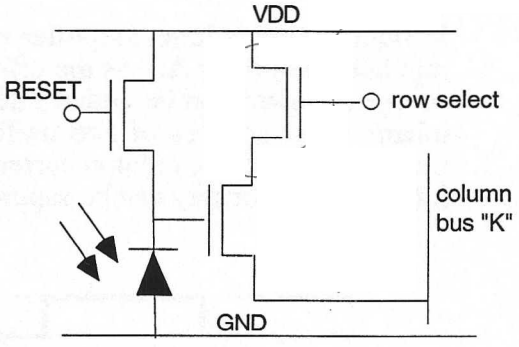

fig. 1 : 3 transistor active pixel.

In fig. 2, the general schematic of the offset-compensating column amplifier and a 2 x 2 pixel array is shown. The method is based on the fact that the amplifier is forced to an imposed output voltage ("DC" in fig. 2) during one of the two states ("signal" & "reference" or "first state" & "second state") by adjusting an internal offset and memorising it. If afterwards the other state is being read, its voltage shifts proportionally to the difference of both. The output signal itself does not contain variations that are of another origin than variations of the amount of light. Many such column amplifiers are connected in parallel to a common output bus.

Fig. 3 shows the various signals that are expected as input and output of such a column amplifier. The "first state" of the amplifier samples the signal level in the amplifier. Switches S1 and S2 are closed, while S3 and S4 are open. The transistor M then acts as an inverting amplifier, of which the output is fed back to the offset control of the unit amplifier A. The offset of A is regulated until the current through S1 is zero. The voltage at the gate of M is now at a level where the current trough M is equal to the current through the current source I. The amplifier memorises this offset level. All this is done during the horizontal blanking time of the imager, for all columns in parallel. After this, the column amplifier is switched to the "second state" with S1 and S2 open and S3 closed. All pixels of the row are reset. The signal at the column lines increases with a voltage proportional to the light level on the pixel, and so does

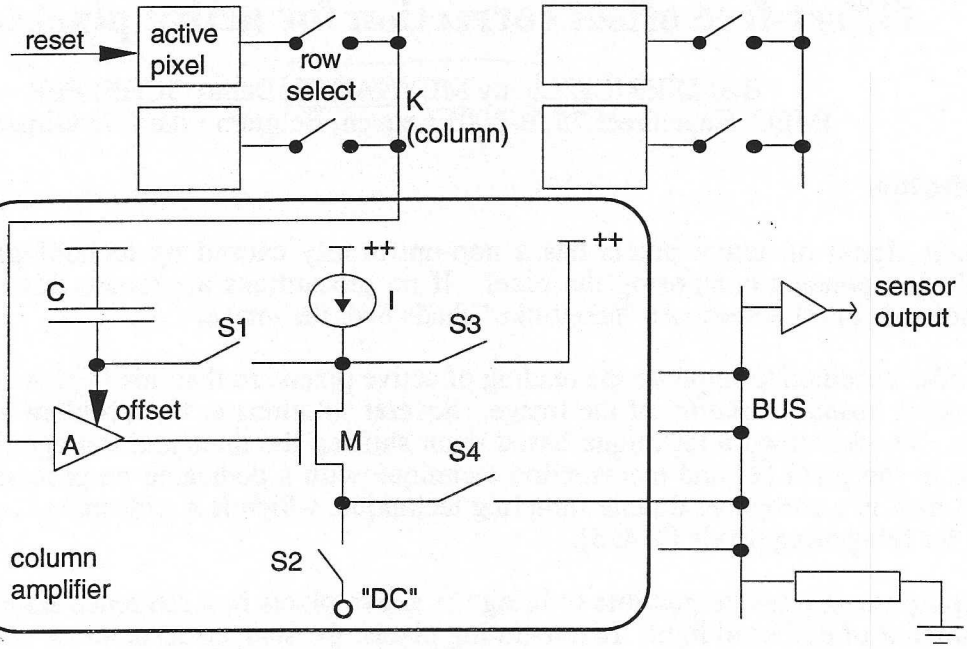

fig. 2 : Schematic operation of a 2 x 2 pixel image sensor, with detail on the column amplifier.

the voltage at the gate of M. When S4 is closed (driven by the vertical pixel clock to read out the row), transistor M acts as a source follower and the photo signal appears also at the source of M. This voltage is shown in fig. 3, and it is free of pixel offsets and of offsets in the amplifier itself.

In figure 4, the column amplifier is shown more in detail, with a particular implementation of the offset-regulated amplifier A. As the offset-regulating element, only a series capacitor was used. Eventually a source follower can be added after the capacitor. The current source I is implemented with a current mirror. The sources of non-uniformity in the amplifier are : the source follower A (if present), the transistor M and the column current source I. Through an adequate implementation of the current source I, this non-uniformity can be suppressed, as will be illustrated by the following analysis.

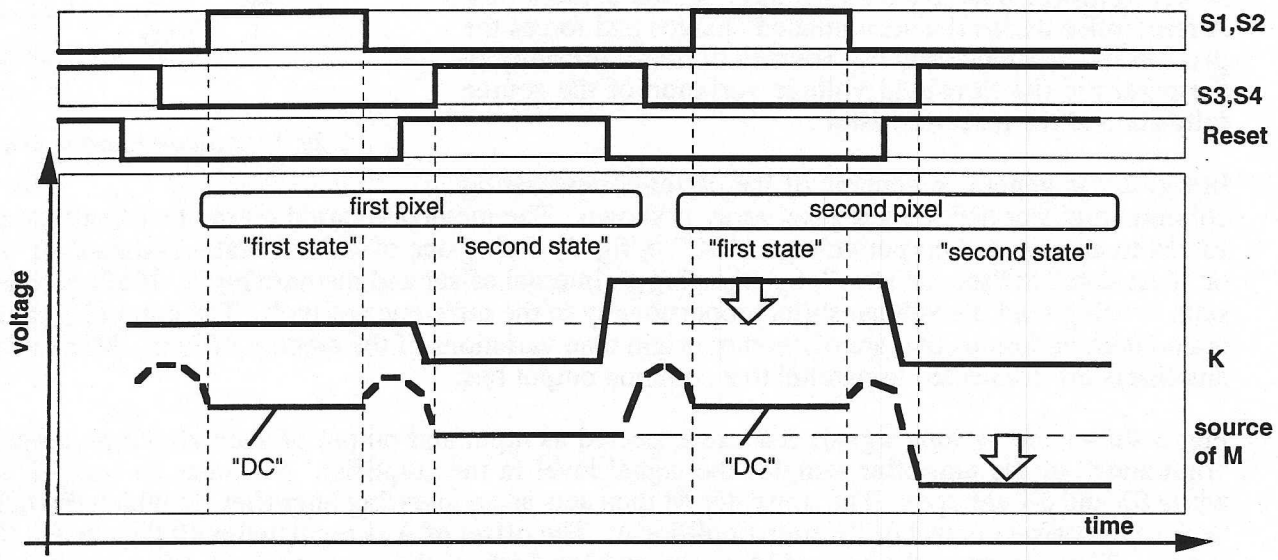

fig. 3 : signals to be expected at key points in the column amplifier while reading two pixels on the same column. Two analog signals are shown: K , the voltage of column bus, which reflects the output of the pixel(s) connected to it, and which is the input of the column amplifier; and the voltage at the source of transistor M, which is the output of the column amplifier. The white arrow indicates the difference of the resulting signal between 2 consecutive pixels.

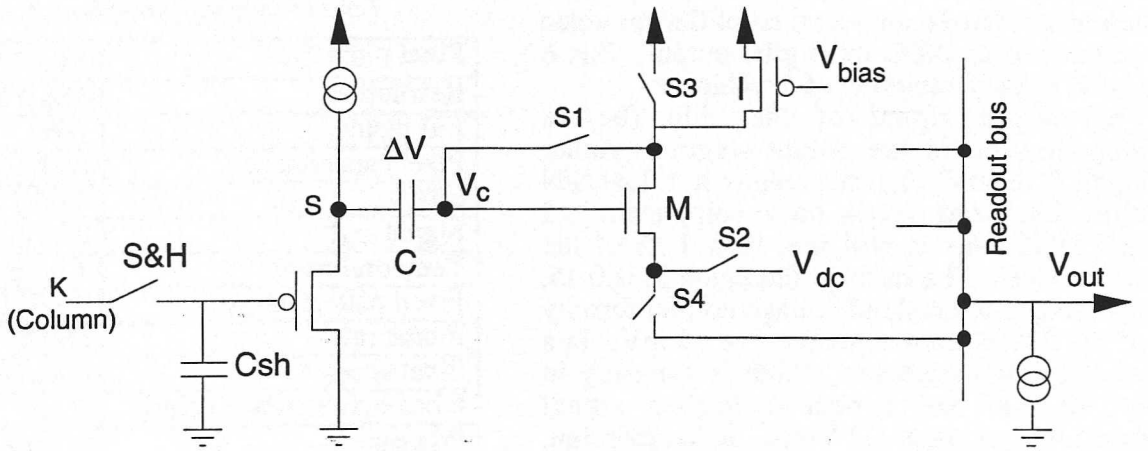

fig .4 : Detail of an actual column amplifier circuit. Signal from the column line K goes to a sample&hold stage. The series capacitor C is charged/discharged trough S1 in the "first state" for offset compensation depending on the non-uniformities and holds this charge during readout. The output signal goes to a common readout bus. S4 is driven by the horizontal shift register.

During the first state, with S1 and S2 closed, the gate voltage of M will be regulated by charging/discharging capacitor C until the current through the drain of M is equal to the current of the current source I. This can be expressed in the following equation, as both transistors are in saturation :

$$K_I' \frac{W_I}{L_I}\left[(V_{bias} - V_{dd}) - V_{th,I}\right]^2 = K_M' \frac{W_M}{L_M}\left[V_c - V_{th,M} - V_{DC}\right]^2 \qquad (1)$$

with V_{dd} the supply voltage, V_{DC} the (externally applied) DC voltage, W & L the width and length of the MOSFETs and $K' = KP/2n$. Index I refers to the current source, and M to the transistor M. V_c is the voltage after the series capacitor. From (1), this voltage can be calculated as :

$$V_c = V_{DC} + V_{th,M} + \alpha \cdot \left(V_{bias} - V_{dd} - V_{th,I}\right) \quad \text{with} \quad \alpha = \sqrt{\frac{K_I' W_I L_M}{K_M' L_I W_M}} \qquad (2)$$

The voltage at node S, after the PMOS source follower which buffers the sample/hold capacitor, is V_{reset}-V_{signal}, with V_{reset} the reset level of the pixel and V_{signal} the voltage swing due to the integration of the photo current. At the end of the first stage, a voltage $\Delta V = V_{reset} - V_{signal} - V_c$ appears over the capacitor C. During the second state, M acts as a source follower. The pixel is reset and the voltage at node S changes to V_{reset}. The output voltage of the source follower can be calculated as :

$$V_{out} = V_{reset} - \Delta V - V_{th,M} \qquad \text{or} \qquad V_{out} = V_{signal} + V_{DC} + \alpha(V_{bias} - V_{dd} - V_{th,I}) \qquad (3)$$

The only varying parameter in the output signal is the threshold voltage of the column current source. But with the right choice for the W/L ratios of the current source and transistor M, the factor α can be kept low. In the current design, an α of 0.023 is used, resulting in a reduction of the column-wise fixed pattern noise to 2.3% of the V_{th} non-uniformity.

3. Implementation in an image sensor

We have implemented this offset-compensation circuit in an image sensor. The architecture is shown in figure 5 and specifications are listed in table I. The right vertical shift register selects the rows which are read out. Pixels are reset by this shift register (to read out the reference signal) or by the left vertical shift register (in case of integration time shortening, to determine the start of the integration period). The horizontal shift register drives switch S4 of the column amplifier which multiplexes the column amplifier output signals on the readout bus. An on-chip video output stage contains a multiplexer for the video

reference signals, an output amplifier for video output and an ADC for digital output. Fig. 6 shows a die photograph of the chip.
The output signal of the chip (before amplification in the output stage) is rather small (273 mV) and this results in a low S/N ratio. The fixed pattern noise component is 2 mV RMS, this is still less than 1 % of the signal level. The factor α (equation 3) is 0.15, resulting in a threshold voltage non-uniformity of the PMOS current source I of 14 mV. In a redesign of the sensor, which is currently in processing, we expect a higher signal amplitude, of about 1.2 Volts. In the redesign, α is 0.023, which should result in a even lower non-uniformity of 0.3 mV.

Table I : specifications of the APS image sensor

Pixel pitch	14 x 14 μm^2
Resolution	386 x 290 pixels
Fill factor	16%
Pixel capacitance	60 fF
S/N	44 dB
Signal sat	273 mV
Temporal noise	1.87 mV RMS
Fixed pattern noise	2 mV RMS
Frame rate	50 Hz
Pixel speed	8 MHz
# bad pixels (white spots)	< 50
Process	0.7 µm CMOS

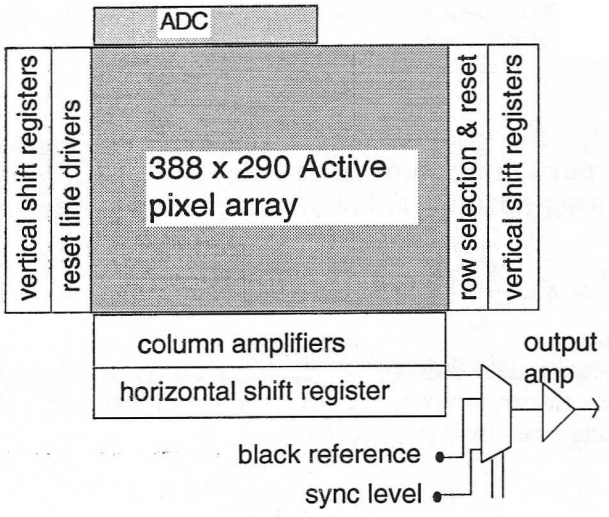

fig. 5 : architecture of the active pixel sensor

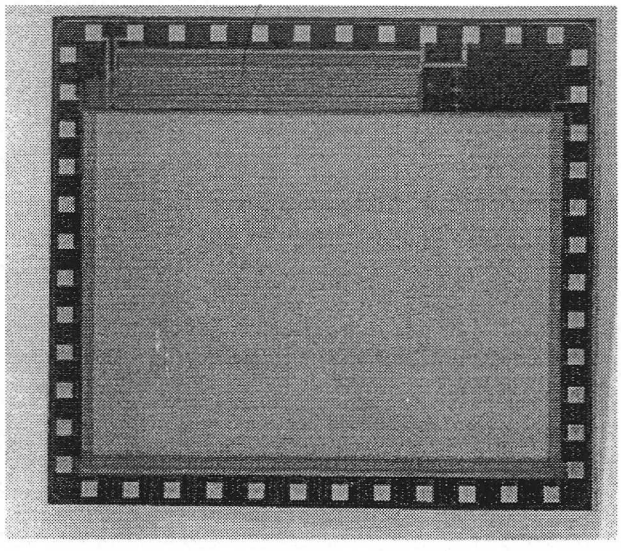

fig. 6 : die photograph of the image sensor

4. Conclusions

An offset-compensating amplifier was described. The amplifier performs correlated double sampling to tackle the fixed-pattern noise problem in an active pixel CMOS image sensor. The amplifier also compensates its own non-uniformities and is demonstrated in a 386 x 290 pixels image sensor.

5. References

[1] N. Ricquier, B. Dierickx, "Active pixel CMOS image sensor with on-chip non-uniformity correction", proc. IEEE Workshop on CCD & AIS, Dana Point, April 20-22, 1995
[2] B. Dierickx, D. Scheffer, G. Meynants, W. Ogiers, J. Vlummens, "Random addressable active pixel image sensors", proc. Spie vol 2950, pp. 2-7, Berlin, 1996
[3] R.H. Nixon et al, "128x128 CMOS photodiode-type active pixel sensor with on-chip timing, control and signal chain electronics", proc. Spie vol. 2415, pp. 117-123, San Jose, 1995
[4] D. McGrath, V. Clarck, P. Duane, L. Mcllrath, W. Washkurak, "current-mediated, current-reset 768x512 active pixel sensor array", proc. ISSCC, vol.40, pp. 182-183, San Francisco, 1997
[5] B. Ackland, A. Dickinson, "Camera on a chip", proc. ISSCC, vol.39, pp. 22-25, San Francisco, 1996