An In-situ Storage Image Sensor (ISIS) with Elongated CCD Storage for a High-speed Video Camera of One Million PPS

Takeharu Etoh and Kohsei Takehara

Kinki University, Higashi-Osaka 577, Japan.

1. BACKGROUND TO ISIS

The authors developed a 4,500-pps high-speed image sensor in 1992 which utilized a 16-channel parallel readout[1]. This paper presents a new In-situ Storage Image Sensor (ISIS) with full parallel processing.

Parallel processing is common practice in high-speed electronic processing, the ultimate expression of this being the simultaneous processing of all elements. Processes in moving image capture with a video camera include photoelectric conversion, signal storage and reproduction of images from the stored signals. Since reproduction can take place after image capture has ended, an image sensor which simultaneously processes photoelectric conversion and storage of all pixels at a reasonable speed is the ultimate high-speed image sensor. Each pixel of the image sensor has at least one photoelectric converter, usually a photodiode, and signal storage to record consecutive images. The authors, therefore, call this type of sensor ISIS, or in-situ storage image sensor. The acronym also happens to be the name of the most important goddess in Egyptian mythology.

2. POTENTIAL PERFORMANCE AND TECHNICAL CONSTRAINTS OF ISIS

If the number of storage elements required per pixel, and hence the number of frames recordable by the device, is less than 10, an existing high-speed imager, i.e. an image converting multiframing camera, can be used instead of the ISIS. However, if the number of storage elements is less than 50, such a device cannot reproduce moving images since there are simply not enough frames to give a sensible playback time. In this case, the images are effectively a sequence of stills.

A larger pixel size would provide the space required for more storage elements, but the total chip size is limited and larger pixels reduce the total pixel count and so the resolution. It follows that it is important to manage the inverse relationship between the total number of frames and the resolution. A minimum resolution may be 256×256 pixels, and in practice the maximum chip size is about 20×20 mm having a photo-receptive area of 15×15 mm surrounded by control circuits. The pixel size is then 55×55 μm (15,000/256).

If ten seconds of replay at the normal NTSC frame rate of 30 pps is considered the minimum requirement, then 300 frames must be stored. If a triple-sensor video camera is employed, the number of frames required for each sensor is 100. When the storage elements for each pixel are placed inside the pixel, the size of each element is 5.5×5.5 μm (55/10), which is not difficult to achieve with current IC fabrication technology.

In the above discussion, the area of the photodetector associated with each pixel is ignored. There is a trade-off between the areas required for the photodetector and storage elements of each pixel, i.e. between the sensitivity and number of frames. Some techniques are available to augment the light sensitivity, for example attaching micro lenses, increasing illumination, direct attachment of an image intensifier, and the deposition of an avalanche layer on the photodetector. On the other hand, tripling the number of sensors is just about the only way to increase the number of frames. Increasing the number of sensors beyond a factor of three lowers the sensitivity and makes the camera too bulky to be of practical use. Therefore it is better to allocate more area to the storage elements and less to the photodetector, resulting in a storage element size slightly less than the estimate of 5.5×5.5 μm above.

When a CCD is employed as the storage device, three wires must be fabricated within the width of each storage element to drive the charge, so sub-micron fabrication is necessary to manufacture an ISIS suitable for the capture and reproduction of moving images.

3. PREVIOUS ISIS PROPOSALS

3.1 ISIS with parallel CCD storage

An ISIS proposed by Kosonocky (shown in Fig. 1) was actually fabricated and proved the validity of the ISIS approach by capturing 30 consecutive images at 833,000 pps. He refers to it as a burst image sensor, but the current authors classify it as an ISIS with parallel CCD storage.

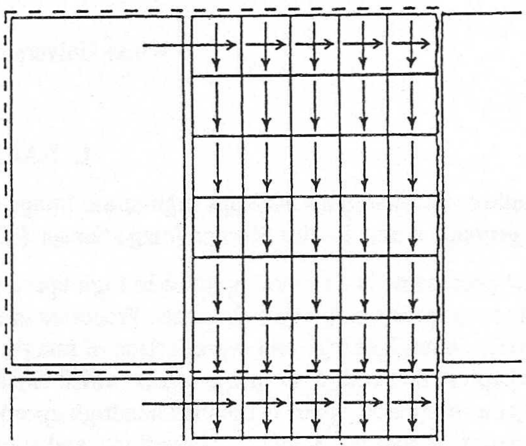

Figure 1 ISIS with parallel CCD storage proposed by Kosonocky

3.2 ISIS with staggered photo-sites

A conventional frame-transfer CCD covered with a light shield having open slits. Sixteen consecutive frames can be captured at the rate of charge transfer on the vertical CCDs. This type of sensor has been fabricated by some manufacturers, but the vertical resolution is reduced to one-sixteenth of the horizontal. Howard, Gardner and Snyder[2] modified the design, as shown in Fig. 2, by aligning the photo sites in a staggered configuration to give the same resolution in both horizontal and vertical directions. They succeeded in capturing 16 consecutive images at one million pps, with the single direction change significantly improving the image quality.

The sensor still has some disadvantages:

(1) The fill ratio is less than 6% and is reduced inversely as the total frame count is increased, which makes it difficult to develop the sensor for a video camera having more than 100 frames.

(2) It is difficult to build an overwriting mechanism which facilitates synchronization of image capture with the occurrence of a target phenomenon.

4. PROPOSED ISIS WITH ELONGATED CCD STORAGE

4.1 Elongated CCD storage

The authors have sought the simplest possible ISIS configuration, each pixel having a straight CCD storage path with no bends. All the ISISes proposed so far, except the one produced by SMD and the US Air Force, seem to contain the same design approach whereby the storage elements associated with each pixel are confined within the area of the pixel itself. To achieve this, the storage CCD has to be folded or divided into several parallel strips. On the other hand, if a straight CCD "hanging down" from a pixel were to be employed, it would pass through the next several pixels as shown in Fig. 3a. The problem in this case is to arrange the pixels and the straight storage CCDs such that the square light-receptive area is filled and so has no vacant space. The authors refer to this straight CCD storage as elongated CCD storage.

4.2 Overlaid ISIS with elongated CCD storage

To simplify the explanation of the proposed configuration and its operation, an overlaid ISIS with elongated CCD storage is shown in Fig. 3a,b and used as an example.

One pixel of an overlaid CCD image sensor is covered by a photodetector and the CCDs for charge transfer are buried beneath the photodetector. The photodetector for the next pixel is connected to the CCD column to the right, and so on for subsequent pixels. When viewed as a column of pixels, the lines of storage CCDs underneath fill the available area, as shown in Fig. 3a,b. Operation during the image capture and readout phases is different and described below.

(1) Images capture phase

The electric charge generated in the photodetector is sent down to a CCD element (indicated by a dot in Fig. 3a,b) and then transferred along the CCD storage elements. When it reaches the last element (indicated by a circle), it is drained through the base of the sensor chip. To prevent the charge from being transferred further along the strip, and so interfering with the storage area for another pixel, the electric potential of the boundary element (indicated by a triangle) is kept high. The overwriting operation continues until a target phenomenon is observed and a trigger signal received, halting the overwriting.

(2) Readout phase

The transfer of charge from the photodetectors to CCD storage, and drainage through the base are stopped. The electric potentials of the boundary elements are controlled to allow electric charge to pass.

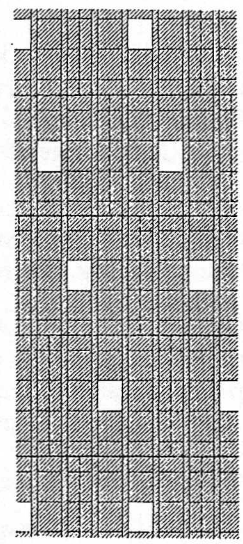

Figure 2 ISIS with staggered photo-sites by Howard, Gardner & Snyder

An ISIS with elongated CCD storage has the following strong advantages.

1) Image signals are transferred in one direction only during the high-speed image capture phase, and the wires required to drive the charges are fabricated in a single layer. This simplified fabrication process with no bends in the charge path minimizes the degradation in image quality.

2) The CCDs perform the dual roles of storage during the image capture phase, and of charge transfer during the readout phase. The entire photo-receptive area, therefore, is completely utilized to store image signals.

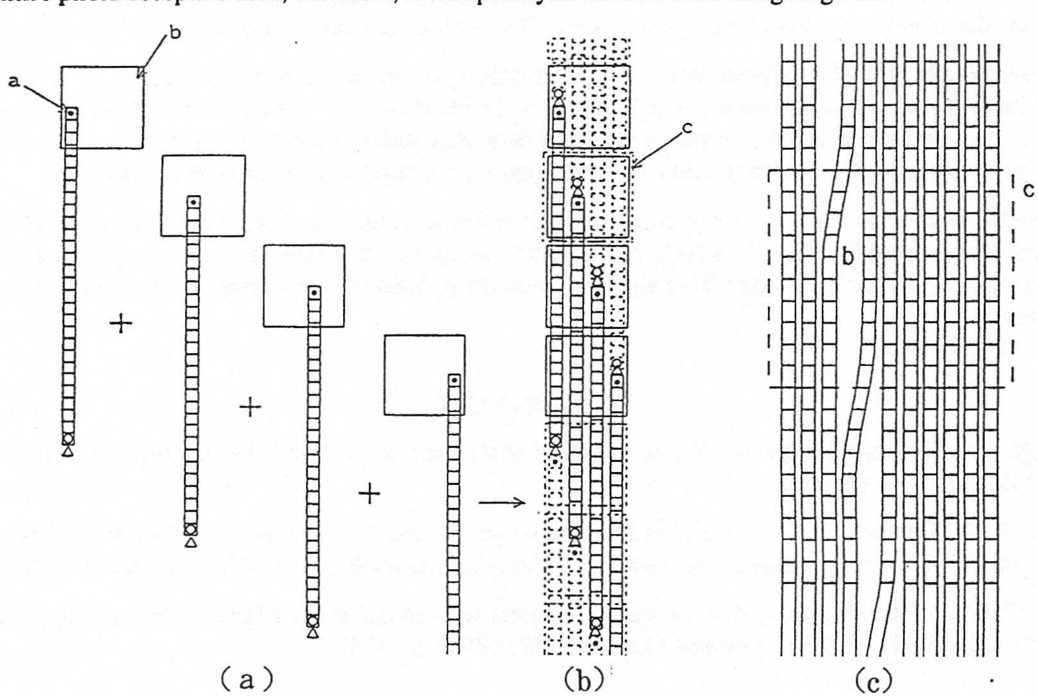

Figure 3 ISIS with elongated CCD storage by the authors

a. CCD storage, b. photo detector, c. pixel

It is very difficult, however, to transfer electric charge from the photodetector directly to the top of a CCD element, so in a practical design the charge should first be transferred down to a gate fabricated on the same plane as the CCDs and, then, transferred to the first element of the CCD storage for that pixel. Therefore, it is necessary to make space available for the gate between adjacent CCD storage columns.

It would be possible to increase the distance between columns and place the gates for column of pixels in the resulting gaps, but this wastes space. To avoid this, a small modification is introduced where adjacent CCD columns meander slightly in a staggered manner (see Fig. 3c) and the small spaces so introduced are used for the gates.

If the degree of curvature introduced into a column can be kept small, it is expected that charge will still be able to flow without leaving significant residual charge at the meanders, which could cause degradation in image quality such as ghosting. The knife-shaped space can also be used for additional circuits to support other useful functions as well as the gate, such as charge drainage and video triggering (explained later).

4.3 Plane ISIS with elongated CCD storage

The knife-shaped space between CCD columns is also used for the photodetector. The configuration is referred to as a plane ISIS or an interline ISIS with elongated CCD storage.

The fill ratio, i.e. the ratio of the gap to the overall pixel area, is around 10% for a 100-frame-storage CCD. In this configuration, the fill ratio decreases inversely with the square root of the total frame count. A micro cylindrical lens can be attached to each photodetector, which leads to an actual fill ratio of more than 20%.

5. VIDEO TRIGGER

Synchronization of the stop of the overwriting operation in the image capture phase with the occurrence of a target phenomenon is a serious problem in high-speed image capture, especially when the total number of frames is not large, a characteristic of ISISes. As the image signals are not read out in real time during image capture, a device is required which can monitor the occurrence of the target phenomenon. The authors proposed the following video trigger in 1992[3].

The light-receptive area of an ISIS is divided into $n \times m$ large blocks, in which n and m are in the range 3 to 5. Suppose $n = m = 4$, then there are sixteen large blocks. The intensity of the incident light on each of the 16 blocks is monitored by reading out the data in parallel and converting it to digital data. Any sudden change in intensity in some blocks indicates a change in the state of the subject, and a trigger signal is generated to stop the capture operation.

The simplest way to generate such a trigger signal is to deposit an amorphous silicon layer, containing an embedded 10×10 μm grid of aluminum wires forming 4×4 large blocks, onto the glass cover of the image sensor package. This produces the electrical signal for the trigger. This approach provides a video trigger system, which is essential to ISISes, built into the sensor.

REFERENCES

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