Anti-Blooming Optimisation using Simulations & Measurements for a VAB Process

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A semiconductor CCD process is described which provides vertically integrated electron blooming barriers using a patterned P-Well in n-substrate. The optimisation of the electronic performance of this structure depends critically on the process and in particular the P-Well design. This paper reports on the use of state-of-art process simulation tools together with experimental data to determine the best means to optimise the device design. A schematic cross-section through the structure of a simple pixel is shown in Figure 1a, together with a potential profile along a vertical line through the pixel centre in Figure 1b. The photo-generated electrons collect at the potential minimum in the buried channel and in normal operation are read out to a charge sensing structure by manipulating the gate potentials. The direction of charge motion is perpendicular to the page. This investigation deals with the behaviour of the electrons in the pixel during charge integration, during which time the gate potentials are effectively constant. When sufficient photo-generated electrons are collected, they begin to fill up the available storage capacity in the pixel. If they reach the surface of the pixel, blooming and CTE issues may 'contaminate' the signal in adjacent pixels. With the structure shown in Fig 1a, the vertical barrier is designed to be lower at the pixel centre to ensure that excess electrons are drained away to the substrate before this happens. This is referred to as vertical anti-blooming (VAB) [1].

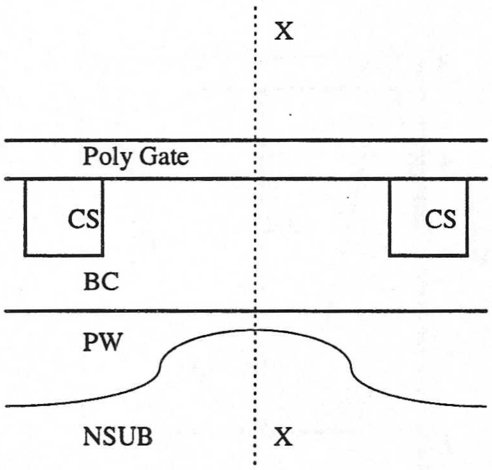

Figure 1a. Schematic cross-section through a simple pixel. BC = buried channel, CS = channel stop, PW = P-well.

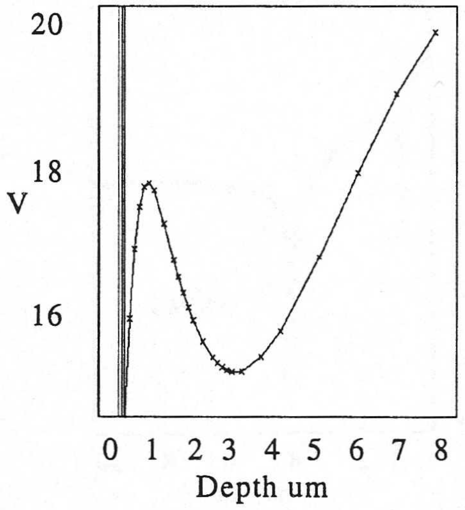

Figure 1b. Schematic of potential profile along the line XX through the pixel centre.

The use of simulation tools [2] reduces the amount of experimentation required to determine the optimum process parameters. The simulation allows the selection of an optimal set of implants to maximize the pixel full well capacity and anti-blooming performance. These results are then used to define a set of processing experiments. The results from these wafer runs are then used to improve the simulation accuracy and allow extrapolation to different pixel designs. The first steps in calibrating the process simulations are as follows: starting with a 1-dimensional calibration, where the simulated doping profile is matched with measured (SIMS) data, an example is shown in Figure 2a. Then, the simulated channel potential of a simple FET-like structure (4.7V) is matched with measured channel potential in a FET fabricated in a continuous P-well with BC implant (4.5V+/-0.2V); the potential profile for this structure is shown in Figure 2b.

The potential profile shown in Figure 2b illustrates a vertical barrier with a height of about 3.2V. The continuous PW implant used for this structure shows the surface potential well above the barrier potential and hence no vertical anti-blooming. In order to implement an anti-blooming effect, the potential barrier is lowered at the pixel centre by tailoring the PW dose. This can be achieved by masking the pixel centre during the implant (P-well gap) and using a thermal process to diffuse the implant to the pixel centre. This effectively increases the net BC doping at the pixel centre and reduces the PW barrier height, the combination of which gives rise to an increased channel potential and reduced barrier height. The target for the process is to achieve a barrier voltage just above the surface potential, such that charge packets are drained over the barrier before reaching the surface. The height of the channel potential peak reflects how much charge may be stored in the pixel and defines another parameter for optimisation.

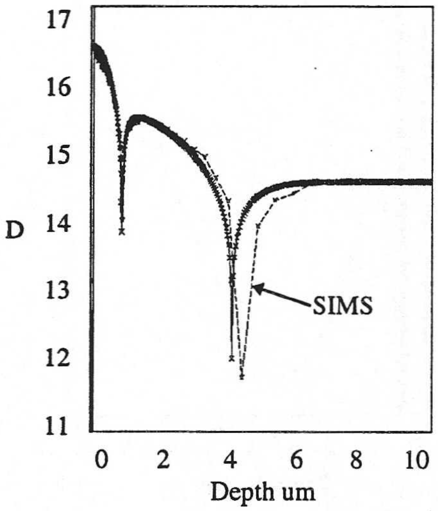

Figure 2a. Simulated and measured (SIMS) doping profile long a line normal to the wafer surface, D = Doping Density.

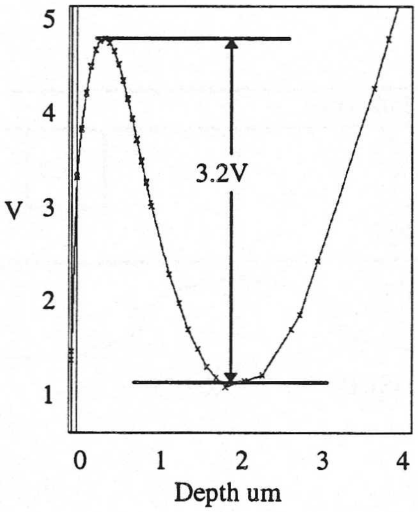

Figure 2b. Simulated potential profile for blanket P-well and BC implants, showing a barrier height for signal electrons of 3.2V.

The P-Well dose at the centre of the pixel is varied to demonstrate the effect of this on the potential profile. This can be achieved by varying either the P-Well gap or the implant dose. For this investigation, it proved easier to vary the implant dose and a common P-Well gap used throughout. The simulated effect of varying P-Well dose by +10% and -10% from the optimum value is shown in Figure 3a. The consequence of increasing the P-well doping is a higher potential barrier, which leads to a larger full well capacity. The change in the simulated potential profile with different BC implant dose is shown in Figure 3b. The effect of increasing the BC dose is an increase in the full well capacity. However, as BC is increased, it compensates for the P-well implant and reduces the blooming barrier which acts to reduce the full well capacity. Hence, it is the inter-dependence of the BC and P-well implant doses that determine the behaviour of the pixel. The thermal budget for the process is just as important as the dose levels. This budget is often determined by other requirements of the process and hence is not a variable.

A number of wafers were processed with different implant doses to investigate this behavior experimentally. Using the DALSA IA-D6-0512 sensor [3] as a test device, a 512 x 512 frame transfer area array operating at a nominal data rate of 25 MHz. The results, shown in Table I, are consistent with the trends indicated by the simulation results.

Table I. Video Saturation Level

P-well implant dose	BC implant dose	Video Saturation Level
optimum	optimum	100 %
- 10 %	- 8 %	90 %
- 23 %	- 8 %	55 %
- 16 %	+ 12 %	28 %

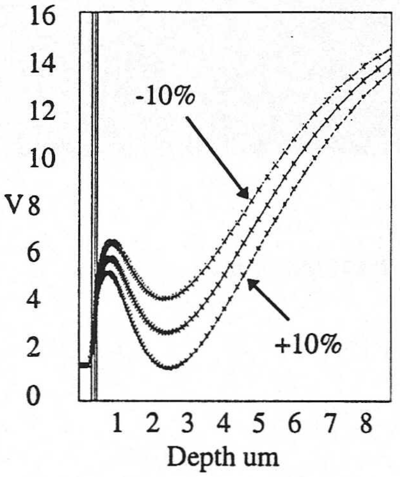

Figure 3a. Simulated potential profile through pixel centre with optimum BC implant and P-well implant +/- 10% of optimum.

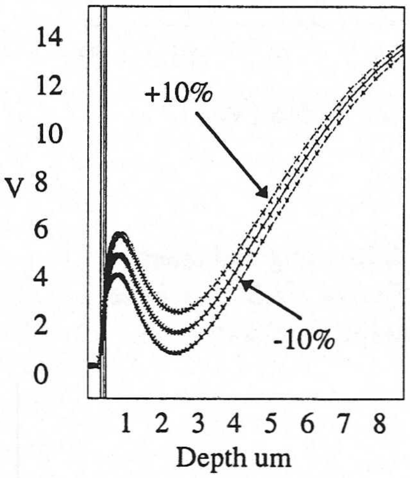

Figure 3b. Simulated potential profile through pixel centre with optimum P-well implant and BC implant +/- 10% of optimum.

The potential profile is also a function of the applied substrate bias (NSUB) which can be used to fine tune the behavior of the pixel. This enables the Full Well capacity to be reduced in favour of stronger antiblooming performance or vice versa. Data was obtained from the IA-D8 sensor for a number of different VNS biases. The results, shown in Figure 4a show how the saturated video output level (related to full well capacity) increases as VNS is reduced, and how the VAB performance increases as VNS is reduced. The VAB performance is measured by illuminating the sensor through an aperture mask with a diameter of 10% of the sensor size. The illumination is adjusted to saturation (just before the onset of blooming) and then increased until the image size doubles in diameter as a result of blooming. The degree of over-illumination with respect to the saturation equivalent illumination is deemed to be the anti-blooming level. An antiblooming level of 100x means that the sensor requires 100x the saturation level of exposure to double the image size of a bright spot. A typical image is shown in Figure 4b.

In conclusion, we have shown the results of simulations and demonstrated how they may be used to optimise the process used in a Vertical Anti-Blooming process. This significantly reduces the spread of process split experiments required to determine the optimal process.

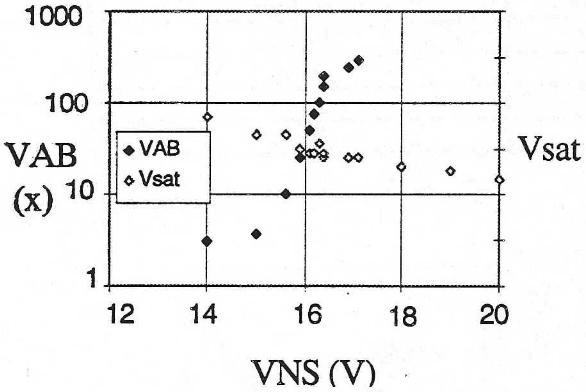

Figure 4a. Antiblooming and video level as a function of VNS bias. Note the log scale on the VAB axis.

Figure 4b. Example image.

References

[1] Albert J P Theuwissen, "Solid-State Imaging with CCDs", Kluwer Academic Publishers, (1995).

[2] SILVACO, process simulation tools ATLAS, ATHENA, TONYPLOT, DEVEDIT, DECKBUILD.

[3] DALSA Databook, p155, (1996-7).