A High Responsivity Photodetector on SOI Substrate

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Introduction:

Silicon-On-Insulator (SOI) technology has long been used in military, aircraft, space systems and other applications under hazardous conditions. It has also received much attention in the commercial market recently due to its potential to produce CMOS circuits with higher performance, reduced power consumption, lower production cost and higher yield [1]. Because of the nearly perfect isolation in SOI technology, different types of devices can be integrated easily. The integration of photodetector and CMOS circuit on SOI substrate can find many applications including large scale space navigation system, and low cost, low power imaging systems with both detector array and image processing circuitry on the same chip. However, traditional photodetectors, such as CCD array and photodiodes are very difficult to fabricate on SOI substrate because the silicon film available is usually below 2000Å. In this paper, we present a high responsivity photodetector using SOI MOSFET operating in the lateral bipolar mode. It has been shown that using normal Lateral Bipolar Transistors (LBT) on bulk silicon can produce optical sensors that are ten times as responsive as identically sized vertical bipolar phototransistors [2]. By utilizing the higher current gain of LBT mode in SOI CMOS technology, photodetector with responsibility about one hundred times of typical photodiode has been demonstrated. The operation voltage required by the proposed photodetector is only about 0.1V, which is ideal for low power applications, which SOI technology is targeted for.

Experiment:

The SOI photodetectors used in this experiment were fabricated on single implanted SIMOX wafers from IBIS Co. with silicon thickness of 2000Å and buried oxide thickness around 1100Å. The process is a typical N^+ polysilicon gate Non-Fully Depleted (NFD) SOI NMOS process [3], thus is not optimized for photodetection purpose. Nevertheless, it shows that the photodetectors developed in this paper can be easily incorporated into any existing SOI CMOS process without the addition of processing burden. The final silicon film thickness and gate oxide thickness are 1650Å and 84Å respectively. The schematic structure is shown in Fig. 1. When the NMOSFET is used as photodetector in the LBT mode, the gate is left floating. The optical illumination that shines on the base of the LBT generates electron-hole pairs, which results in base current. This base current is magnified by the current gain β of the LBT, and thus giving a large drain current as the output signal.

Experimental Results:

The output drain current characteristic of the SOI LBT under illumination is shown in Fig. 2. The current saturated at V_D equal to 0.1V, which is the voltage required to operate the device for sensing optical signals. As a result, ultra low power operation is possible. The output current is less linearly dependent on the absorbed optical power as shown in Fig. 3. The curves in Fig. 3 take the shape of an exponential function as the absorbed power is plotted in logarithmic scale. The amount of photocurrent generated also dependent on the channel length (or base width of the LBT) as shown in Fig. 3 and Fig. 4. As the channel length is reduced, the current gain β increases and gives higher amplification. To have a large output signal and high responsivity, smaller channel length should be used as shown in Fig. 4 and Fig. 5. However, as the channel length decreases, the dark current also increases because the reverse leakage current of the collector-base junction is also amplified by the same β. When the channel length is shorter than 0.3μm, some slight punchthrough is observed in the technology used, as shown in Fig. 6. This results in a sharp increase in dark current, which is undesirable. Therefore, extremely short channel devices should be avoided for the purpose of photodetection.

The absorption process also has a strong dependent on the wavelength of the incident light and the silicon film thickness. The spectral response of the photodetector is shown is Fig. 7. With the technology used to fabricate the photodetector, the maximum response occurs at a wavelength of 500nm.

Discussion:

A more detail examination reveals that the current gain obtained in SOI NMOSFET can be much higher than conventional LBT. This can be attributed to the presence of the N+ polysilicon gate, which results in a vertical band bending at the silicon film. The electrons and holes generated by the incident photons are separated by the vertical electric field in the depletion region. The electrons are driven to the front gate and then swept to the drain along the gate oxide and silicon interface. The holes, on the other hand, accumulate in the body as shown in Fig 1. This results in an increase in the body potential and leads to the bipolar turn-on [4]. The barrier between source and body (or emitter and base) for the electrons near the buried oxide interface is given by:

$$\psi_{BE} = \phi_{bi} - V_{BS} - \phi_c$$

where ϕ_c is the potential different between the front and back gate due to the vertical banding. ϕ_{bi} is the build-in potential of the source-body junction, V_{BS} here can be regarded as photo-induced equivalent body-source bias. On the other hand, the barrier for holes accumulated in the neutral body is only

$$\psi_{BE} = \phi_{bi} - V_{BS}$$

That means the device behaves like a hetero-junction BJT [5][6]. This property results in a different photo-response characteristic from common phototransistors.

MEDICI simulation is carried out to study the operation of the device. The simulated output drain current versus drain voltage behavior under illumination is shown in Fig. 8. The simulation result is similar to that obtained from the measured data and the saturation voltage is also around 0.1V. For comparison purposes, a common Lateral BJT with the same structure as in Fig. 1 except for the absence of the polysilicon gate has been simulated. The simulated output response under illumination is shown in Fig. 9. The incident light in the simulation is adjusted so that the same intensity of an optical signal is shined onto the silicon film and is absorbed. Comparing Fig. 8 and Fig. 9, it can be observed that the current of NMOSFET operated in the LBT mode is much larger than that of common LBT under the same illumination. The presence of the N+ polysilicon has a strong impact on the output current.

The MEDICI simulated vertical potential distribution in the body of the SOI MOSFET is shown in Fig. 10. Unlike regular BJT, which has a flat band across the cross-section of the device, there is a band bending alone the vertical direction. This band bending is responsible for separating the optically generated electron-hole pairs. The electrons moved towards the gate oxide, where the electron barrier between the source and body is much smaller than that at the silicon/buried oxide interface. The holes, on the other hand, will be depleted from the surface, leading to more injection of electrons from the source along the neutral body. As the holes observe a higher barrier at the neutral body compared to the electrons at the gate oxide and silicon interface, a hetero-junction behavior is observed.

In the MEDICI simulation, it is reasonable to assume the amount of base current generated is given by the optically generated carriers [7]. Fig. 11 shows the simulated output current versus equivalent base current. While the β for common LBT is around 10, it is over 100 for MOS LBT. It should be noted that due to the hetero-junction behavior in the MOSFET LBT, ψ_{BE} is no longer constant along the source/body junction and it is dependent on the light intensity. The β here, given by I_C/I_B, bears a different physical meaning as compared with that given by conventional BJT theory. This high current gain is responsible for giving higher responsivity compared with a photodiode (no gain device) [8].

The above discussion provides a general picture on the operation of the MOS LBT photodetector. However, in order to calculate drain current accurately, ray-tracing should be employed to take into account the polysilicon gate, gate oxide and buried oxide thickness as well as spectrum distribution and different absorption coefficient.

When implementing such detectors in the chip, large W and small L are necessary to obtain a high output current. The smallest L is limited by lithography. With the development of advanced lithography system, the photodetector can be scaled with technology. Some layout strategy can be applied to provide area efficient scheme while optimizing the output. An example is the zigzag gate structure given in Fig. 12. From the figure, it can be seen that zigzag gate can have a very significant area saving compared with the straight gate implementation with the same width.

References

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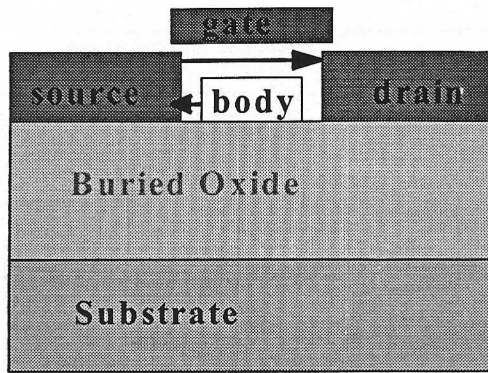

Fig.1 SOI NMOSFET structure diagram

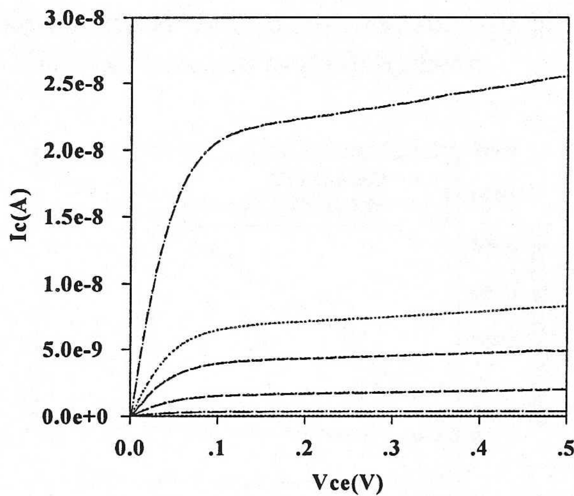

Fig.2 photo-current characteristic of SOI NMOS in Lateral Bipolar mode (W/L=10μ/0.4μ), illumination intensity is 46, 17, 5.6, 2.1, 0.53mw/cm^2 downwards

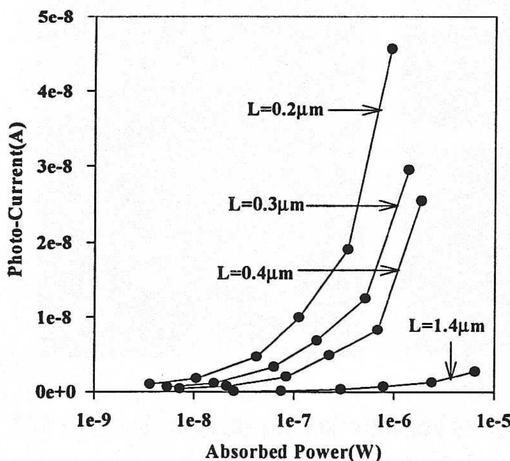

Fig.3 output photo-current versus absorbed power for SOI NMOSFET in Lateral Bipolar Mode (Vds=0.5V), floating body and gate condition

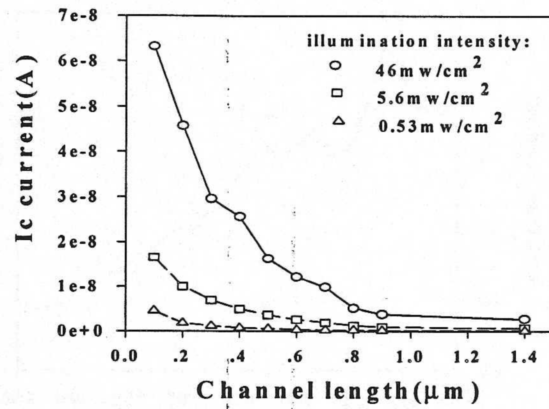

Fig.4 channel length dependent photo-current Ic of SOI NMOSFET(W=10μm, Vds=0.5V) under floating gate and body condition

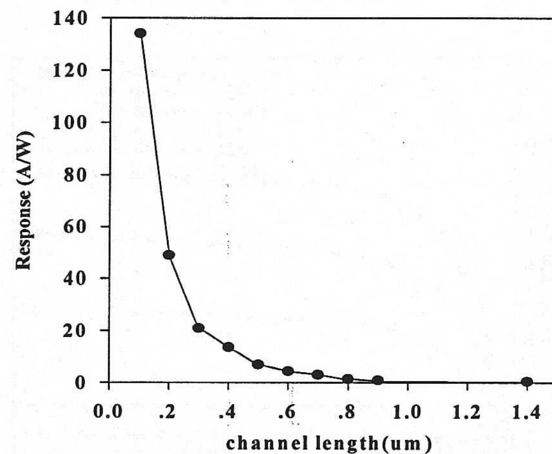

Fig.5 channel length dependent optical response of SOI NMOSFET(W=10μm,Vds=0.5V, 47mw/cm^2 illumination)

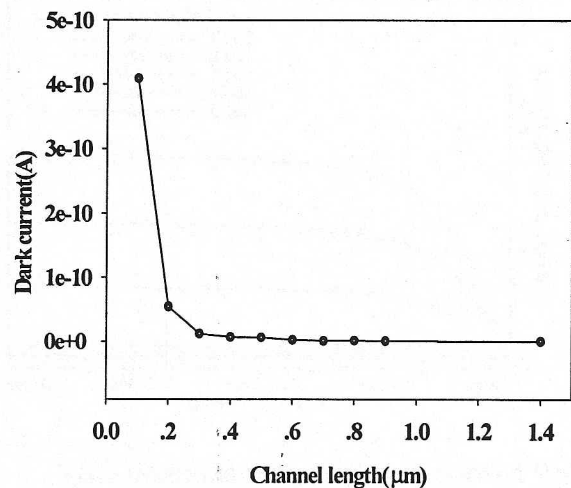

Fig.6 channel length dependent dark current for SOI NMOS(W=10μm,Vds=0.5V)

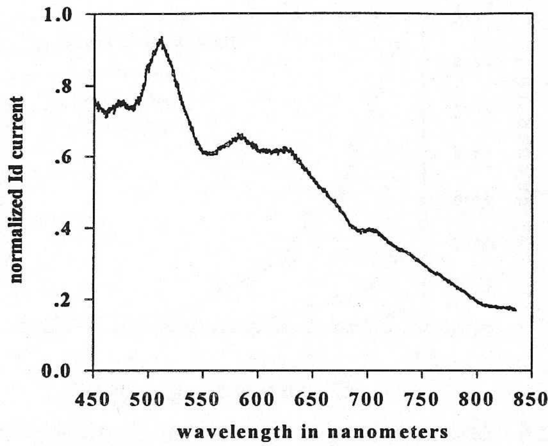

Fig.7 spectra response of the detector in SOI NMOSFET's lateral bipolar mode (Vds=0.5V, floating body and gate)

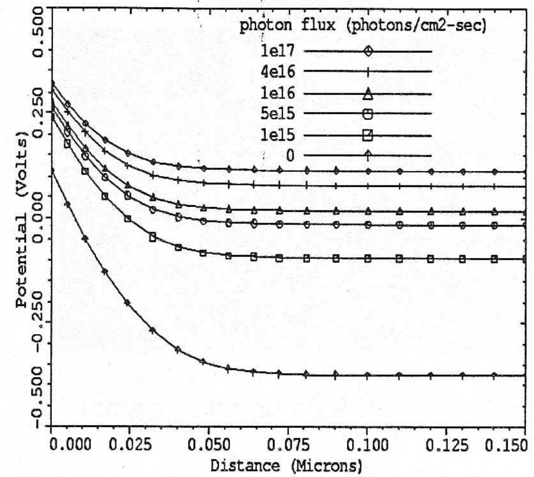

Fig.10 body potential of SOI NMOS in LBT mode(W/L=1μm/0.6μm, Vds=0.4V)

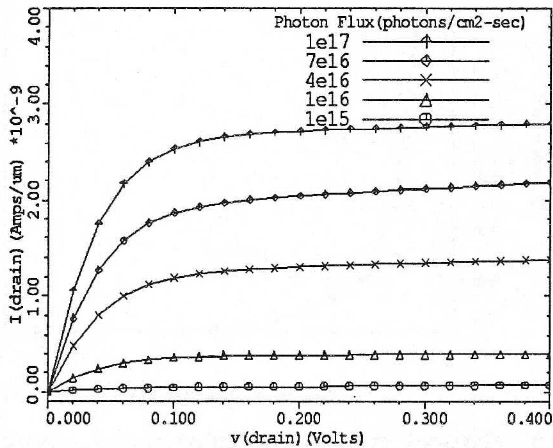

Fig.8 Medici simulation for SOI MOSFET's LBT mode photo-current(W/L=1μm/0.6μm)

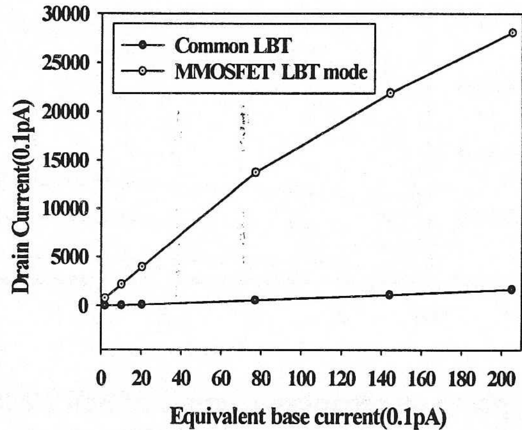

Fig.11 Medici simulation of drain current versus equivalent base current

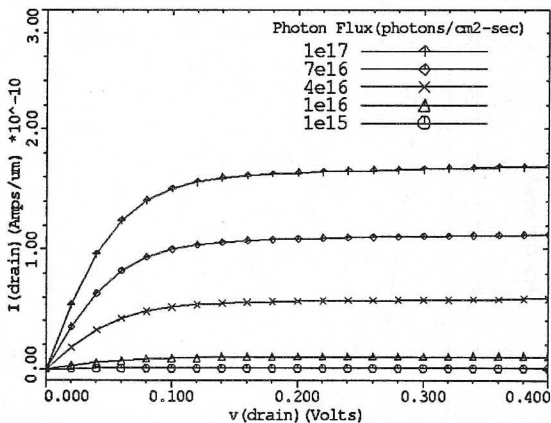

Fig.9 Medici simulation for common LBT photo-current(W/L=1μm/0.6μm)

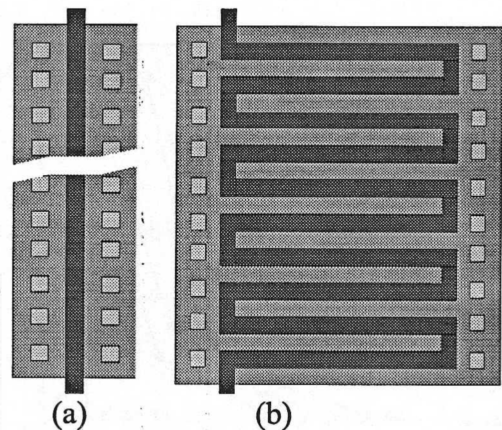

Fig.12 schematic layout design for $W=151\lambda$, λ is the minimum structure size
(a) area=$151\times7\lambda^2$ for straight gate
(b) area=$21\times22\lambda^2$ for zigzag gate