Logarithmic-Converting CCD Line Sensor and Its Noise Characteristics

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1. Abstract

A logarithmic-converting CCD line sensor incorporating logarithmic-converting circuits which utilizes MOSFET's subthreshold operation has been developed. The sensor has 2240×3 pixels that are 12μm×12μm. It outputs a signal logarithmically proportional to the integrated amount of the incident light over more than five orders of magnitude in intensity. The random noise characteristics of the sensor is reported. The S/N value of the sensor is maintained more than 40dB down to an incident illuminance of 0.1 lux.

2. Introduction

The performance of CCD image sensors has made a great progress, especially in shrinking the chip size and in increasing the resolution. But in terms of dynamic range, there still remains a problem to be solved. CCD image sensors have suffered from poor dynamic range compared with a human eye and even with a silver-halide film.

We have developed a newly-conceived CCD line image sensor that has a dynamic range of over more than five orders of magnitude in intensity of the incident light. The sensor incorporates logarithmic-converting circuits for every pixel, which is comprised of MOSFET's and utilizes their subthreshold operation.

The logarithmic-converting CCD image sensor enjoys the wide dynamic range and can take bright objects and dark objects at the same time. It also requires no iris diaphragms and illumination control.

Furthermore, as the sensor outputs a signal logarithmically proportional to the integrated amount of the incident light, its output signal is proportional to the densities on the prints or the films. That means that the digital data converted from the sensor output signal retains the image quality in the dark part as well as in the bright part. It provides excellent artifact-free pictures with no contouring and no visible quantization using 8-bit component.

3. Principles of the Logarithmic Conversion

The logarithmic-converting CCD image sensor employs MOSFET's not only for output amplifiers but also for logarithmic-converting circuits. The logarithmic-converting circuit is comprised of MOSFET's and utilizes their subthreshold operation.

A MOSFET is a four-terminal (gate, source, drain, and substrate) device. The threshold voltage is a gate voltage above which drain current flows from the drain to the source. But even when gate voltage is below the threshold voltage, some drain current called the subthreshold current flows. The logarithmic-converting CCD image sensor exploits this inherent characteristics of a MOSFET.

In the subthreshold region(when V_G-$V_S \leqq V_T$ +nkT/q), if V_D-$V_S \gg$kT/q and surface-state density equals zero, drain current I_D can be written as

$$I_D = I_{D0} \exp\left[\frac{q}{nkT}\left(V_G - V_S - V_T\right)\right] \quad \text{---(1)}$$

$$I_{D0} = \frac{W}{L}\mu_n C_0 \frac{1}{n}\left(\frac{nkT}{q}\right)^2 \exp(-1) \quad \text{---(2)}$$

where

V_G : gate voltage V_D : drain voltage

V_S : source voltage V_T : threshold voltage

W : MOSFET's channel width

L : MOSFET's cannel length μ_n : electron mobility

q : electron charge k : Boltzmann's constant

C_0 : capacitance of gate oxide layer

C_D : capacitance of depletion layer

$$n = \frac{C_0 + C_D}{C_0}.$$

Eq.1 shows that the subthreshold current depends on gate voltage V_G exponentially.

Fig.1 presents an equivalent circuit of a basic logarithmic converter using a MOSFET.

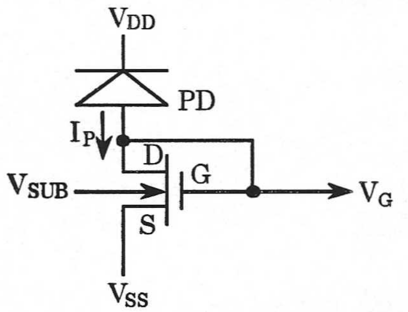


Fig.1. Equivalent circuit of a basic logarithmic converter.

In Fig.1, since $V_D = V_G$ and $I_D = I_P$, from Eq.2 photocurrent I_P is given by

$$I_P = I_{D0}\exp\left[\frac{q}{nkT}\left(V_G - V_{SS} - V_T\right)\right] \quad \text{---}(3)\ .$$

From Eq.3, it follows that

$$V_G = V_{SS} + V_T + \frac{nkT}{q}\ln\left(\frac{I_P}{I_{D0}}\right) \quad \text{---}(4)\ .$$

From Eq.4, it is shown that photocurrent I_P is logarithmically converted to a gate voltage V_G.

4. Logarithmic-Converting Circuit

To avoid the fluctuation caused by the illumination and to increase the signal to noise ratio, integration is indispensable to the logarithmic-converting image sensor as well as the linear image sensor. So, we have introduced an integration circuit for the logarithmic-converting circuit as shown in Fig.2.

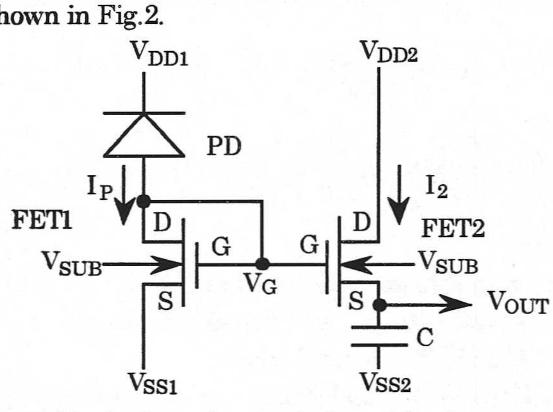


Fig.2. Equivalent circuit of a logarithmic converter connected with a integration circuit.

In Fig.2, if FET1 and FET2 have the same characteristics, since the current flow into FET1 equal I_P, from Eq.4 V_G can be written as

$$V_G = V_{SS1} + V_T + \frac{nkT}{q}\ln\left(\frac{I_P}{I_{D0}}\right) \quad \text{---}(5)$$

and from Eq.1 the current flow I_2 into FET2 is given by

$$I_2 = I_{D0}\exp\left[\frac{q}{nkT}\left(V_G - V_S - V_T\right)\right] \quad \text{---}(6)$$

and the current flow into capacitance C equal I_2, it follows that

$$I_2 = C\frac{dV_{OUT}}{dt} \quad \text{---}(7)\ .$$

From Eq.5,6,7 the following relation is obtained:

$$C\frac{dV_{OUT}}{dt} = I_P\exp\left[\frac{q}{nkT}\left(V_{SS1} - V_{OUT}\right)\right]$$

and therefore

$$\exp\left[\frac{q}{nkT}\left(V_{OUT} - V_{SS1}\right)\right]dV_{OUT} = \frac{I_P}{C}dt \quad \text{---}(8)\ .$$

Integrating

$$\int_{V_{OI}}^{V_{OUT}}\exp\left[\frac{q}{nkT}\left(V_{OUT} - V_{SS1}\right)\right]dV_{OUT} = \int_0^t \frac{I_P}{C}dt$$

yields

$$V_{OUT} = V_{SS1} + \frac{nkT}{q}\ln\left\{\frac{q}{nkTC}\int I_P dt + \exp\left[\frac{q}{nkT}\left(V_{OI} - V_{SS1}\right)\right]\right\} \quad \text{---}(9)\cdot$$

The last term is negligible when $V_{OI} \ll V_{SS1}$, therefore

$$V_{OUT} \cong V_{SS1} + \frac{nkT}{q}\ln\left(\frac{q}{nkTC}\int I_P dt\right) \quad \text{---}(10)\ .$$

Eq.(10) represents the output voltage Vout of the logarithmic-converting circuit. This equation shows that Vout is logarithmically proportional to the integrated amount of the incident light. Note that Vout is proportional not to the integrated amount of the logarithmic value of the incident light but to the logarithmic value of the integrated amount of the incident light. This is a very important feature of this circuit because we can get a proportional value to the integrated amount of the incident light easily by converting the output value to exponential.

5. Pixel Structure

Fig.3 presents the diagram of each pixel including the logarithmic-converting part shown in Fig.2. The above-described integration circuit is merged into the CCD shift register to simplify the device structure. In Fig.3, DC voltage V_{SS} is applied to the source of FET1, DC voltage V_R is applied to the second electrode of the CCD. Furthermore, shift clock F_S is applied to the third electrode of the CCD, and transfer clock F_1 and F_2 to the fourth and the fifth electrode. Whereas, charge injection clock F_D is applied to the charge injection diode of the CCD. In this diagram, the charge injection diode corresponds to the drain of FET2 in Fig.2 , and the potential well under the second electrode corresponds to the source of FET2 and the capacitor in Fig.2.

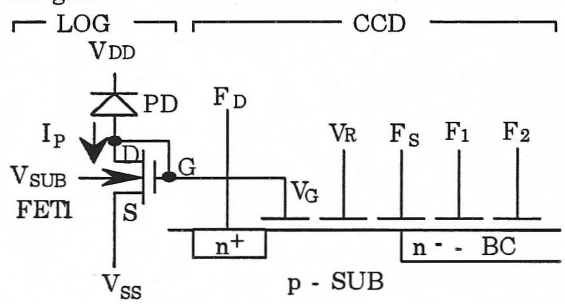


Fig.3.Diagram of the logarithmic conversion part .

A cross-sectional view of the pixel is shown in Fig.4, where

1: p type silicon substrate 2: n- well region
3: p+ region forming photo-diode cathode
4: n+ region which V_{DD} is applied to
5: p+ channel stop region
6: n+ region forming the drain of FET1
7: n+ region forming the source of FET1
8: poly-silicon layer forming the gate of FET1
A: aluminum photo-shield layer .

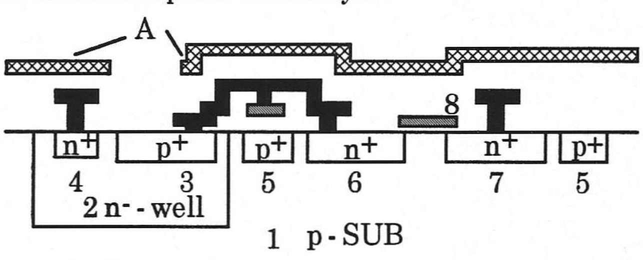


Fig.4. Cross-sectional structure of the logarithmic conversion part .

6. Device Operation

Fig.5 shows the timing diagram for the clock waveforms to operate the image sensor, and Fig.6 presents the potential diagrams of the pixel at selected times. Gate 9 corresponds to the gate of the second MOSFET in Fig.2. Gate 11, which is biased at a DC voltage V_R, corresponds to the source of the same MOSFET and the capacitor in Fig.2.

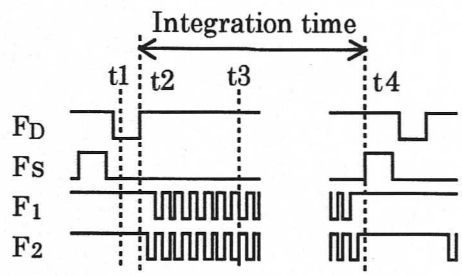


Fig. 5. Timing chart of the device.

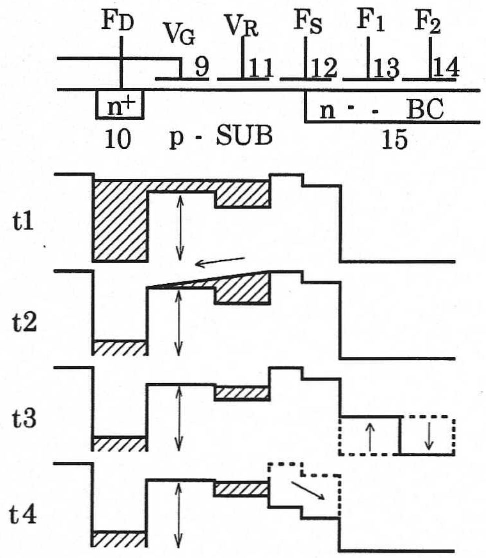


Fig.6. Potential diagrams corresponding to times t1 through t4 of Fig.5 .

7. Device Structure

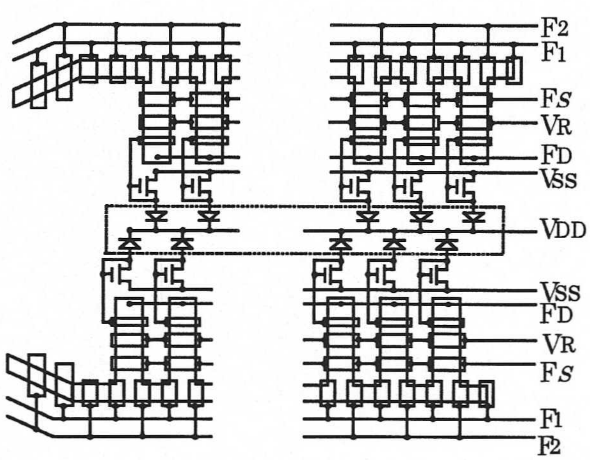


Fig.7. Diagram of one channel of the device .

The image sensor consists of three parallel line photodiode arrays, each with 2240 photosites for the output of R, G, and B signals, and with logarithmic-converting circuits and CCD shift registers for the both sides.

Fig.7 shows a detailed diagram of each line. Each photosite has a size of 12 μ m × 12 μ m. Each MOSFET has a channel length of 12 μ m and a channel width of 10 μ m. The center to center spacing of the photodiode arrays is 768 μ m.

8. Device Performance

Fig.8 illustrates the photoconversion characteristics of the device. It can be seen that the device outputs a signal logarithmically proportional to the integrated amount of the incident light over more than five orders of magnitude.

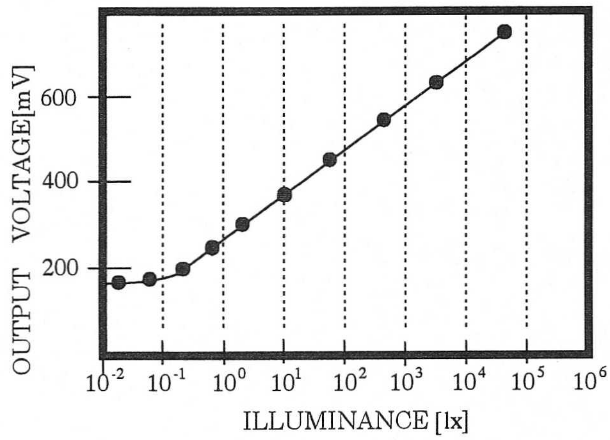


Fig.8.Photoconversion characteristics of the device .

Photo.1 presents a reproduced image by a camera-type scanner incorporating the device. The image was taken under the following conditions: F 5.6, integration time is 5.12msec/line, 3200 line scan, the ratio of the brightness between the darkest part and the brightest part is about 30,000.

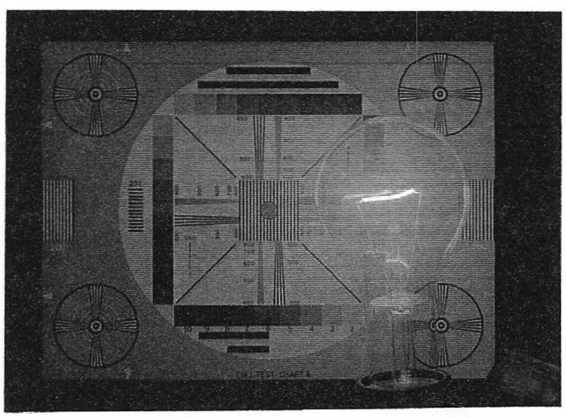
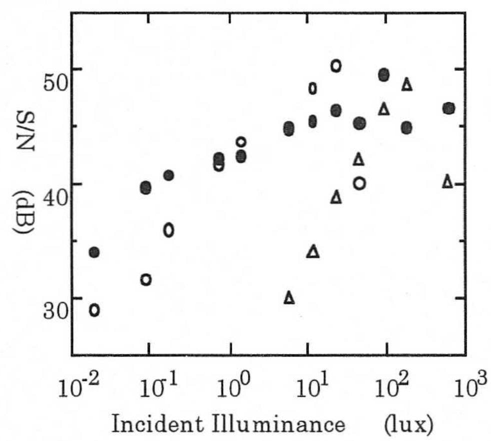


Photo.1. Example of reproduced image .

9. Random noise characteristics

We studied the random noise characteristics of the sensor. We measured the signal-to-noise-ratio (S/N) at the output of the sensor(Fig.9). The result shows that the S/N value of the sensor increases slowly as the incident illuminance increase. It means that the S/N value of the sensor is maintained more than 40dB, which is practically enough, down to an incident illuminance of 0.1 lux. It seems that this causes from the suppression of the shot noise by the logarithmic-converting circuits. On the contrary, in a conventional CCD, the S/N value increases more rapidly, reaching a peak value, and then decreases as the incident illuminance increase. As a result, the S/N value of the conventional CCD is maintained more than 40dB for less than two orders of magnitude of the incident illuminance.



● Logarithmic-Converting CCD
○ Conventional CCD (integration time: 1/60sec)
△ Conventional CCD (integration time: 1/1000sec)

Fig.9. S/N of the Logarithmic-Converting CCD and a conventional CCD

10. Conclusions

We have developed a logarithmic-converting CCD image sensor. It has been demonstrated that the device has a wide dynamic range of over more than five orders of magnitude, and its output signal is logarithmically proportional to the integrated amount of the incident light. It is expected that this technology will be very useful and versatile for digital copiers, camera-type scanners, and film scanners, as well as other new applications.

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