cancelled

LEAKAGE CURRENT REDUCTION OF LARGE-AREA SILICON MICROSTRIP SENSORS

Wen-Chin Tsay, Yen-Ann Chen, Li-Hong Laih, Jyh-Wong Hong, Augustine E. Chen[1], Willis T. Lin[1], Yuan-Hann Chang[1], Suen R. Hou[1], Jyh-Dong Tang[2], Chung-Hsin Chio[2], Song-Tsang Chiang[2] and Hsien-Jen Ting[3]

Department of Electrical Engineering, National Central University, Chung-Li, 320, Taiwan, R.O.C.

[1]Department of Physics, National Central University, Chung-Li, 320, Taiwan, R.O.C.
[2]Suntek Electronics Inc., 20, R&D Rd II Science-based Industrial Park, Hsin-Chu, Taiwan, R.O.C.
[3]Miracle Technology Co. Ltd., 6F-7, No.472, Guang-Fuh Rd., Sec. 1, Hsin-Chu, Taiwan, R.O.C.

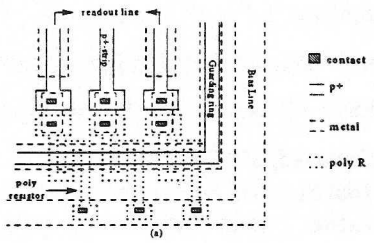
Abstract -- *The 8x4 cm^2 single-sided silicon microstrip sensors with coupling capacitors and polysilicon bias resistors were fabricated with the planar technology. In this paper, we describe different methods to reduce leakage current of silicon sensors. Several gettering technology has been studied to remove the impurities and defects from active region. A LOCOS (local oxidation of silicon) isolation process had been used to reduce the side-wall leakage of sensor. Also, the Sirtl etch analysis of sensor revealed that the side-wall leakage current would be caused by the implantation defects. Several annealing techniques had been studied to remove the boron-implantation damage. The fabricated prototype sensors had been tested at the CERN SPS area. The test results showed that such a sensor is feasible.*

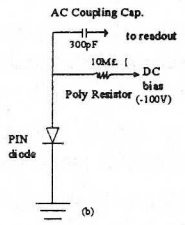
I. INTRODUCTION

Experiments in high-energy physics require not only accelerators to provide particles for the interactions, but also detectors to determine what happens during the interactions. Due to the silicon microstrip sensor has the fast response and high-precision spatial resolution, it has been used or proposed to be used for vertex detection and tracking in many existing and future experiments of high-energy physics [1]-[2]. For improving the S/N (signal-to-noise) ratio during detection, how to reduce the leakage current of a large-area sensor was the most major concern recently. Several special device designs have been also investigated to reduce the leakage current coming from sensor [3] or strip [4] edge. Our studies found the device leakage current was dominantly caused by the boron-implantation damages [5], [6]. This paper presents the results of our studies related to the gettering technology, isolation process and several methods to prevent from implantation damage.

II. SAMPLE PREPARATION

The p^+-i-n^+ silicon microstrip sensor was fabricated on a 4-inch 4 kΩ-cm n-type (111) silicon wafer with a 32015μm thickness. This sensor was single-sided, single-metal, with direct-bias resistors and AC-coupling readout capacitors, and needed 4 masks [5], [6]. These masks were used to define the p^+-strips, polysilicon resistors, contact holes and metal strips. The sensor size (8x4 cm^2) was chosen to maximize the device sensitive and rectangular area on a 4-inch wafer. The layout of one corner of silicon microstrip sensor and the equivalent circuit of the sensor are shown in Figs. 1(a) and 1(b) respectively. The microstrip sensor consisted of p^+-i-n^+ diode strips. The strip pitch was 25 μm, whereas the readout pads, located near the two edges of the sensor by turns, were in two parallel columns with a pitch of 50 μm. Each diode was connected to a bias bus with an individual polysilicon biasing resistor. The resistance of polysilicon resistor was chosen to be 10 MΩ so that the larger device leakage current caused by irradiation during detection did not significantly reduce the reverse-biased voltage on the p^+-i-n^+ diode by an amount of the incremental voltage drop on the bias resistor. The coupling of the metal readout line to the diode was capacitively through a multi-layer dielectric - oxide-nitride-oxide (ONO). Due to its nearly pinhole-free characteristics, it was expected the ONO capacitor had the higher breakdown voltage and production yield than those of the usual oxide capacitor [5]. The other terminal of metal readout line was ended with a bonding pad of area of 70 x 200 μm^2. A guard ring was employed to reduce the dark current of the sensor by decoupling the current generated outside the device active area. This guard ring could also reduce the electric field in the sensor, which otherwise could cause an avalanche breakdown of sensor. The schematic of cross-section profile of sensor is shown in Fig. 1(c).





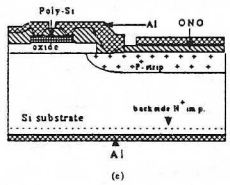


Fig. 1. (a)The layout of the corner of silicon microstrip sensor, (b)the equivalent circuit of silicon microstrip sensor , and (c)the schematic cross-section rofiles of silicon microstrip sensor.

III. REDUCING LEAKAGE CURRENT

A. Gettering techniques

The most popular technique used to reduce the leakage current of semiconductor device is gettering process. In recent years, various gettering techniques have been widely used in VLSI fabrication to remove the impurities and defects from the active regions of semiconductor devices. However, most of these gettering techniques were developed for Czochralski-grown (CZ-grown) silicon wafers. But to fabricate silicon microstrip sensors, the high-resistivity Floating-Zone-grown (FZ-grown) silicon wafers should be used. Therefore, we investigated several gettering processes for the used FZ-grown wafers. The test results are summarized in Table I. The condition G, which was the ERSO's CCD gettering technique combined with backside polysilicon and ONO deposition process, was found be the most effective and suitable one.

Table I. The leakage currents of sensors made with different gettering processes.

Condition	Leakage current(nA/cm^2) under 100V reversed	Remark
A:backside n^+ doped	800-1000	
B:backside polysilicon deposited	200-450	finally, poly removed
C:backside poly & ONO deposited	200-300	finally, poly & ONO removed
D:"high-low-high" heat cycle	1000-1200	modified 3-step gettering
E:condition D with B	800-1000	finally, poly removed
F:"low-high" heat cycle	450-700	modified 3-step gettering
G:ERSO's CCD gettering with C	80-100	finally, poly & ONO removed
H:condition F with A	300-450	
I:condition F with C	150-300	finally, poly & ONO removed

B. Side-wall leakage current

To find the dominant component of device leakage current, several p^+-i-n^+ junction test structures were designed. The large-area square diode was designed to monitor the leakage current due to the bulk junction, and the diode with long-perimeter finger was designed to measure that due to the side-wall junction. By comparing the leakage currents of these two p^+-i-n^+ junction diodes, we found the side-wall one dominated the device leakage current [6].

A LOCOS isolation process which was a modified CMOS poly-gate conventional process was intentionally used to reduce the device side-wall leakage current. The schematic cross-section for sensor made with a modified LOCOS isolation process is shown in Fig. 2. This modified LOCOS isolation and the field implantation could be used to increase breakdown voltage and decrease the side-wall leakage current of the sensor. This modified LOCOS process used a reverse-toned first mask for the p^+-strips in Fig. 1. The leakage currents of sensors made with LOCOS processes are listed in table II and will be investigated and discussed further in the following paragraph.

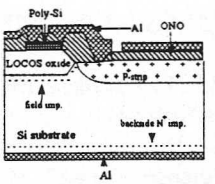


Fig. 2.The schematic cross-section profile of sensor made with LOCOS isolation process.

Table II. The leakage currents of sensors made by LOCOS isolation process.

	Leakage current	
Field implantation	70V reversed	100V reversed
none	> 1 mA*	> 1 mA
P^{31}, 40KeV, $2x10^{13}$	6.93 μA	12.65 μA
P^{31}, 40KeV, $3x10^{13}$	5.22 μA	6.52.5 μA
Fig. 1 process	6.33 μA	8.23.7 μA

*:breakdown at 40-50V, 8-10 μA before breakdow

C. Implantation damage

As could be seen from Table II, only a moderate improvement of sensor leakage current had been obtained with the modified LOCOS process. To obtain the more detailed information, the Sirtl defect etch analysis was employed. Sirtl etch is often used to delineate various crystallographic defects of silicon wafer, such as dislocation and stacking faults. After the wafer was treated with Sirtl-etch solution, the stacking faults that nucleated in the p^+-implantation region were found, but no stacking fault was found in the isolation region, as shown in Fig. 3. This revealed that the side-wall leakage current of the sensor was probably caused by the stacking faults in the p^+-implantation region. These stacking faults would be due to the p^+-strip implantation damages. Since, the implantation damages would be enhanced and might cause slips in Si wafer if the temperature difference along the radius of the wafer was significant during process of fabrication. Generally, there are two approaches to reduce the implantation damages. The first method is to use an alternative doping technology to replace the implantation process. The other one is developing an annealing process to remove the implantation defects. In our studies, the boron solid source predeposition technique had been used to replace the p^+-strip implantation process. A significant improvement of sensor leakage current had been obtained and presented in our earlier report [6].

However, it was difficult to obtain high-purity boron-plus wafer for solid source predeposition process. The impurities in boron-plus wafer still had chance to diffuse into the p^+-strip and generated defects in the p^+-strip. Therefore, several annealing techniques were tested to remove the implantation damages. The relations between the sensor leakage current and annealing temperature for different implantation conditions are listed in table III.

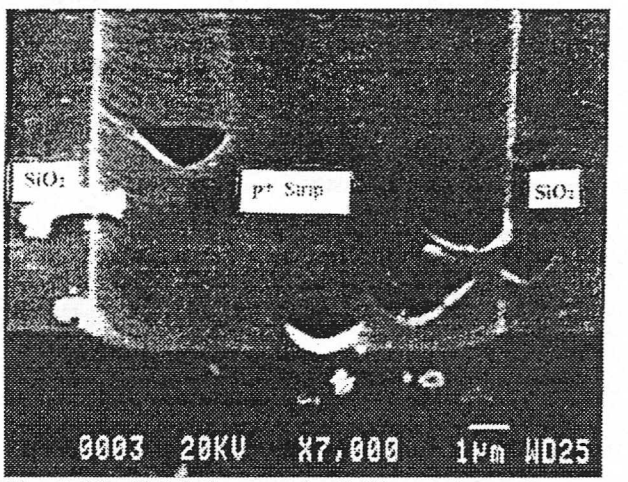


Fig. 3. The SEM photograph of silicon microstrip sensor after Sirtl etch.

The condition of $5x10^{14}$ ions/cm^2 boron implantation with a 900°C annealing was the conventional one of this sensor process. As could be seen the lower the dosage implanted, the higher the leakage current was. This might be due to that the $5x10^{12}$ ions/cm^2 boron implantation was below the critical dose for silicon amorphization, so the defect annealing would be more difficult, and much residual damages were left [7]. The boron with Ar implantation or the BF_2 implantation had a lower critical dose for silicon amorphization, so the needed defect annealing temperature could be lower. From table III, it was also found that the needed defect annealing temperature for boron implantation was 1000 °C, and 800 °C for boron with Ar implantation or BF_2 implantation respectively. The leakage current of sensor made with p^+-strip implantation process and enough defect annealing was lower than those of sensors made with boron solid source predeposition process.

Table IV. A comparision of leakage currents for sensors made with different ion-implantation and annealing conditions.

implantation dose	annealing	leakage	remark

(ions/cm^2)	temperature (°C)	current (μA)	
B,5x10^{12}	1000.00	61.00	many slips
B,5x10^{14}	800.00	51.00	slips(left side) & many pittings
B,5x10^{14}	900.00	31.00	slips & pitting (left side)
B,5x10^{14}	1000.00	13.00	few pittings
B,5x10^{14} + Ar,10^{15}	800.00	16.00	few pittings
B,5x10^{14} + Ar,10^{15}	900.00	15.00	few pittings
B,5x10^{14} + Ar,10^{15}	1000.00	18.00	few pittings
BF_2,5x10^{14}	800.00	14.00	few slips
BF_2,5x10^{14}	900.00	14.00	one slip
BF_2,5x10^{14}	1000.00	16.00	none
BF_2,5x10^{15}	800.00	13.00	none
BF_2,5x10^{15}	900.00	17.00	none
BF_2,5x10^{15}	1000.00	11.00	none
BF_2,5x10^{12}	800.00	29.00	pittings(left side)
boron solid diff.	1000.00	16-20	many pittings

VI. CONCLUSION

Gettering technologies have been studies to reduce the impuries and defects of FZ wafers. The ERSO's CCD gettering technology with backside polysilicon and ONO deposition process was found to be the best one. From the measurement result of special p^+-i-n^+ junction test structures, it was found that the sensor leakage current was dominated by the side-wall one. A LOCOS isolation process had been intentionally used to reduce the side-wall leakage current of sensor. But, due to the stress effect and implantation damages, only a moderate improvement of leakage current had been obtained. The TEM photograph and Sirtl etch analysis of sensor revealed that the side-wall leakage would be caused by implantation damages. Various defect annealing processes had been investigated to reduce the side-wall leakage. From the studies on defect annealing processes after implantation, it was found the implanted dose should be higher than the critical dose necessary to form an amorphous layer. If there was an amorphous layer on the strip region, the need annealing temperature would be much lower due to the solid phase epitaxy.

Several 8 X 4 cm^2 silicon microtrip sensors made with this proposed process as above, were tested at CERN. From the results of beam test at CERN, it was concluded that sensors made by the proposed process had the high S/N ratio, efficiency and spatial resolution [8], [9]. A prototype silicon microstrip ladder containing 8 pieces of 8x4cm^2 sensor has been also tested. Its S/N ratio deteriorated as the ladder length was increased. With a ladder length of 64cm, an S/N ratio of 10 and a spatial resolution of 5 um had been obtained.

ACKNOWLEDGMENT

The authors would like to thank ERSO/ITRI, Miracle Technology Co. and National Central University for their continuous support. This work was partially supported by the National Science Council of the Republic of China under the contracts NSC 83-0208-M-008-047 and NSC 85-2112-M-008-024.

REFERENCES

[1]J. Kemmer, Nucl. Instrum. & Methods A288, pp.282-286, 1990.

[2]L. Evensen et al, IEEE Trans. Nucl. Sci. NS-35, pp.428-431, 1988.

[3]L. Evensen et al, Nucl. Instrum. & Methods,A337, pp.44-52, 1993.

[4]T. Ohsugi et al, Nucl. Instrum. & Methods A342, pp.22-26, 1994.

[5]W. C. Tsayet al, Nucl. Instrum. & Methods A351, pp.463-465, 1994.

[6]W. C. Tsay et al, Jpn. J. Appl. Phys. Vol. 35, Part 1, No. 2B, pp.1077-1081, 1996.

[7]S.M. Hu: J. Appl. Phys., 49, pp.3259-3265, 1978.

[8]Y. H. Chang et al, Nucl. Instrum. & Methods A363, pp.538-544, 1995.

[9]W. C. Tsay et al, IEEE Trans. Nucl. Sci. NS-42, pp.437-440, 1995.