A novel photoswitch image sensor*

R. H. Dyck, J. Pinter, T. Selbo, S. Onishi, D. Xiao
Lockheed Martin Fairchild Systems, Milpitas, CA 95035
L. S. Haynes, Intelligent Automation, Inc., Rockville, MD 20850
H. E. Brown, Wright Laboratories, Tyndall AFB, FL 32403

Abstract

A novel image sensor is described which can detect the time at which any pixel is illuminated by a pulse of light. This type of image sensor is proposed for use in a camera system that includes a sweeping fan beam of light for image capture in three dimensions. The third dimension is determined by triangulation with the aid of the proper timing information. In contrast with previously published work on such a device, which utilizes conventional CMOS integrated circuit building blocks in the unit cell of the image sensor, in this paper we describe a device that utilizes a two-terminal photothyristor as the pickup element and a CCD readout system for scanning. The rationale for using a photothyristor is that the input energy needed to cause switching can be minimized by integrating the sense element with the switching element so as to minimize the switching sense-node capacitance and to avoid the need for a load element having extremely high impedance and low capacitance. The result is a unit cell as small as 57x72um, compared to 200x200um and larger for published designs using the CMOS building block approach. Using what is essentially a CCD process with a minimum number of modifications needed to make the photothyristors, good CCD performance in prototype arrays and good photothyristor performance in discrete devices have been achieved. The reason that full functionality has not been achieved is attributed to problems in the fabrication of the load element tied to the thyristor. Some of the thyristors fabricated switch on with pulses of light having energies as low as 3fJ.

The 3D Camera System

Gruss and Kanade (1, 2) have described a concept for a fast VLSI rangefinder, and reported on the design and operation of a prototype array and prototype camera system. Figure 1 shows a schematic diagram of the system. A camera with a 2D sensor views a scene and a nodding mirror sweeps a laser fan beam across the scene from the side or from the top. The camera has a narrowband filter to pass the laser wavelength and minimize the effect of any ambient light. The camera operates at near video frame rates. This type of camera system could be useful for robotic navigation, and for optical metrology. It requires relatively little computational power to determine the range dimensions, and can be small. They built small prototype arrays (28x32 pixels) with unit cell sizes of approximately 250x250um and 216x216um, respectively.

The way the unit cell functions is illustrated with the timing diagram shown in Figure 2. The unit cell receives a voltage ramp signal that is in phase with the motion of the laser fan beam. At the moment that the laser pulse from a particular scene pixel is sensed and triggers one unit cell circuit, the unit cell must capture and then store the voltage information. This voltage is called a time stamp. At the end of the laser scan, the array is read out.

In the effort reported here, one objective was to develop a much larger array, that is, one with the order of 200x200 pixels. The first was to be developed for indoor navigation and a subsequent one, for limited outdoor navigation. For an array with this many pixels, the cell size is important, and it appeared that a

*Supported in part by NASA Marshall Space Flight Center and Tyndall AFB.

photothyristor/CCD approach would be able to provide a number of attractive features, including small cell size, good fill-factor, fast turn-on, low fixed pattern noise, and good sensitivity. For these applications it was desireable to have a frame rate of at least about 10Hz.

The Unit Cell Design

The simplest unit cell that can provide the required function is shown in Figure 3. A two-terminal photothyristor and a load element form the input stage of the circuit. The output of that stage controls a switch the connects the ramp input to a sampling capacitor which, in this case, acts like a floating source which can be read out into an adjacent CCD register. As shown in Figure 2, at the beginning of a frame period, the supply voltage to the first stage is ramped up to a fixed voltage, and the time-stamp voltage ramp is started. At the end of the frame, the CCD receiving phase is pulsed to a trilevel high voltage, thus forming a charge packet proportional to the time-stamp ramp voltage. During the following frame period, the charge is read out by the CCD. Before the start of the next frame of range imagery, the voltage applied to the first stage is reduced to zero to allow the thyristors to turn off, and then is ramped up at a rate slow enough that they are not switched on by this process.

The I-V characteristics of the thyristor are shown in Figure 4 for the case of no light and for two light levels. For the loadline shown, the device would not switch at the first light level but would at the second.

A 2-phase CCD was selected for the vertical registers because with only two clock busses the unit cell size could be further minimized. The thyristor design was the result of various considerations, including fill-factor, process latitude, during inital development, to control sensitivity and holdoff voltage, and whether to use a vertical or a lateral pnpn structure. It was decided to use a vertical design and to place the bottom junction at a depth of about 4um. This proved to be a satisfactory choice; a number of variations in the process for different experimental wafers, and a number of different layout variations, gave useful reults. Figure 5 shows a schematic cross-section that illustrates the general device integration problem. The p-wells for the CCD and for the thyristors can be different and, ideally one might want each to be as shallow as possible so that the total lateral diffusion associated with these depths allows a minimum spacing, w, between the elements. For reasons of process simplicity, we chose to make both types of wells with an epi layer and to separate them with a deep isolation diffusion.

The Photothyristor Design

Referring to Figure 5, and calling the n-type diffusion the "n-base", in order to achieve the shallow depth of p-well, it was necessary to have a very shallow p-emitter and to have a means for controlling the minority carrier lifetime in the n-base so that the thyristor would have a useful holdoff voltage. A technique was found that has worked quite well; a number of variations of fabricated devices are moderately photosensitive, hold off voltages in the desired range of 5-10V, and can be biased on in less than approximately 100msec. As determined from various sized experimental thyristors, the large perimeter-to-area ratio of the p-emitter in the smallest thyristors helps in achieving these holdoff voltages in such a shallow device.

In order to achieve high sensitivity and fast turn-on, the capacitance of the center junction should be minimized. In this development program we minimized this capacitance for this depth of structure and for a process that does not require additional masking and diffusion. Another design consideration was the objective of having as high a quantum efficiency for the near infrared laser wavelength as possible.

The Unit Cell Layout

Because of the large space required for the thyristor, its n-type isolation diffusion and the power-limiting load FET, the unit cell is too large to be designed with only one stage of CCD register per unit cell. (The long gates would likely cause an unsatisfactory CTE.) Therefore two stages of CCD register are used per unit cell. This is shown in Figure 6. This technique was also used in the output register. The size of the unit cell in this first design is 57x72um.

Test results

To date, highly sensitive photothyristors and functional CCDs have been fabricated in the same wafer. Thyristors have been switched with pulses of light with energies as low as 3fJ. These have a holdoff voltage of approximately 10V. Those that switched below 4V were considered unusable even though they may have been more sensitive. One of the slowest processes in the functioning of the circuit is the resetting of the thyristors to the biased off state. In the case of the most sensitive devices, this resetting process takes approximately 50-500msec. The ultimate sensitivity of arrays with this simple two-terminal thyristor will apparently be determined by the amount of time that is acceptable for this reset process. In order to prevent punchthrough in the rather shallow thyristor, the p-well doping was higher than is normally preferred for the CCD. This optimization required modelling and evaluation of finished devices with different doping levels, and ultimately proved successful.

References

1. T. Kanade et al., A very fast VLSI rangefinder, Proc. 1991 IEEE Internatl. Conf. on Robotics and Automation, pp. 1322-29.
2. A. Gruss et al., A VLSI smart sensor for fast range imaging, Proc. 1992 IEEE Internatl. Conf. on Intell. Robots and Systems, pp. 349-58.

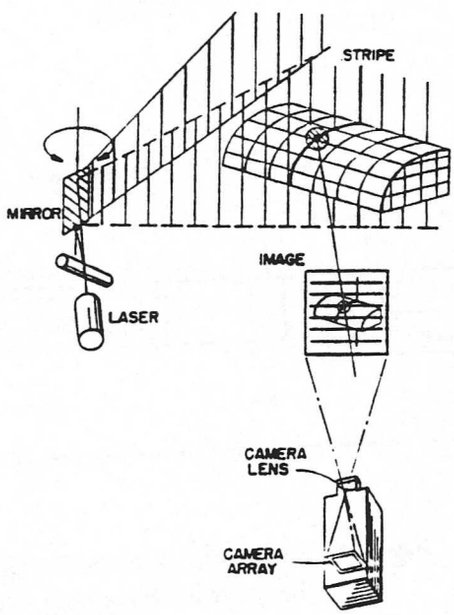

Figure 1. Schematic of 3D camera system

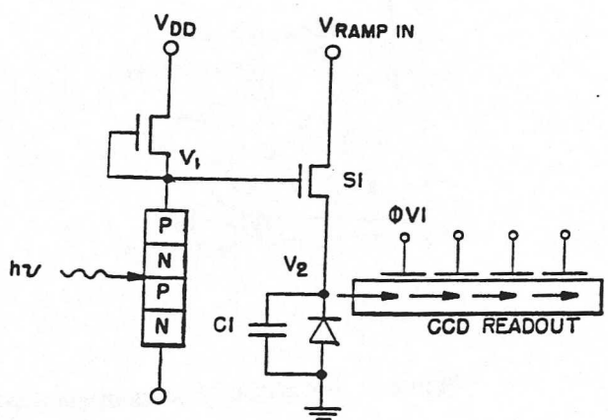

Figure 3. Circuit schematic of the unit cell

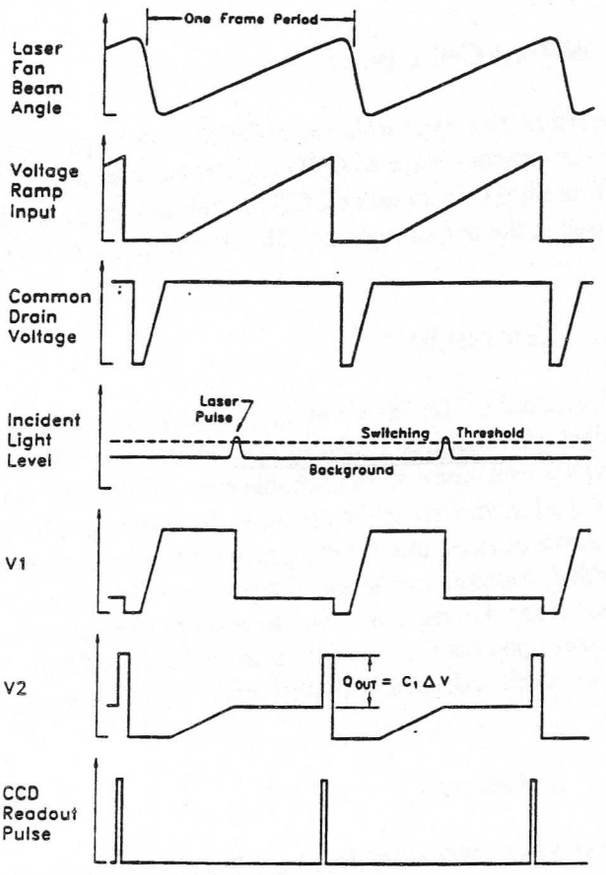

Figure 2. Operation and timing of the camera system

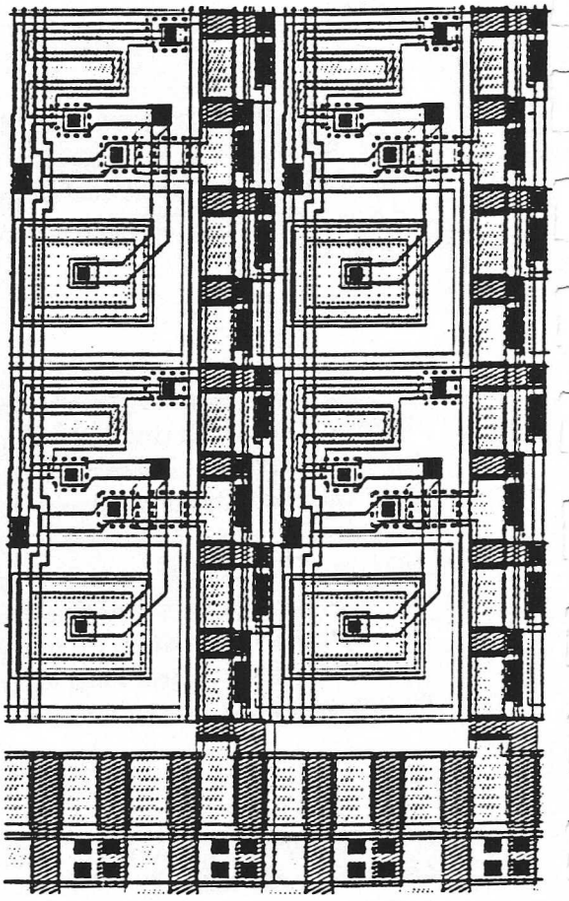

Figure 6. Layout for a 2x2-cell portion of the array

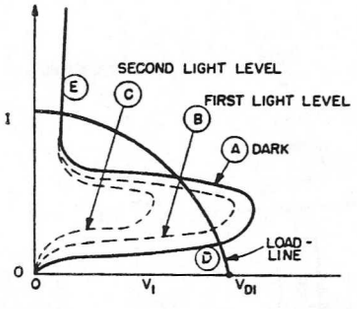

Figure 4. I-V characteristics of the thyristor

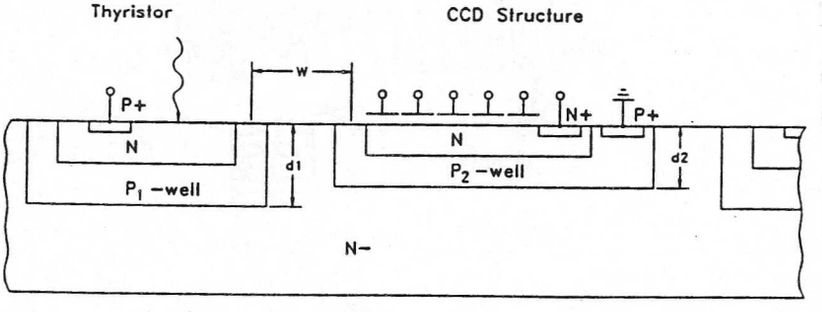

Figure 5. Schematic cross-section showing the general integration problem