Frame-Transfer CMOS Active Pixel Sensor With Pixel Binning*

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Abstract

The first frame-transfer CMOS active pixel sensor is reported. The sensor architecture integrates an array of active pixels with an array of passive memory cells. Charge integration amplifier-based readout of the memory cells permits binning of pixels for variable resolution imaging. A 32x32 element prototype sensor with 24 μm pixel pitch was fabricated in 1.2 μm CMOS and demonstrated.

1. Introduction

The CMOS active pixel image sensor (APS) has permitted the realization of a camera-on-a-chip with high performance [1]. Each pixel contains an active amplifier that buffers the photosignal and drives a column-bus readout architecture. Both photodiode and photogate pixels have been explored [2]. Other CMOS-based active pixels for current-mode readout [3] and logarithmic companding [4] have also been reported. It has been suggested that on-chip frame memory would enhance the ability to perform certain image processing tasks on chip [5] including frame-to-frame difference encoding, motion detection, and variable resolution imaging.

In-pixel memory has been used for motion detection for passive pixels [6], in CMOS APS by a slight change in timing [7], and in more complex compression approaches [8]. In-pixel memory has two major drawbacks. First, retention of data can be deteriorated by both stray light and stray carriers, similar to the origin of smear in an interline transfer CCD. Second, in-pixel memory results in either low fill-factor or large pixels. In this work, a small prototype CMOS APS with separate on-chip frame memory is implemented for the first time to demonstrate the concept and investigate architecture and performance issues. Variable resolution imaging by binning pixels is readily implemented by the architecture. The work represents the first report of a frame-transfer CMOS APS.

2. Sensor Design and Operation

The structure of the sensor is shown in Fig. 1. The full signal chain is shown in Fig. 2. The pixel is implemented as a photogate-type active pixel. Charge is integrated under the photogate and then transferred to the floating diffusion for readout. Row decoder logic on the side of the array is used to select a particular row for readout and apply the proper sequence of signals to enable correlated-double-sampling readout. The exact sequence has been well reported previously [2]. The pixel delivers two sequential voltage signals to the vertical column bus - a reference (reset) level and a signal level. The difference of these two voltages levels is proportional to the charge integrated under the photogate according to the conversion gain of the floating diffusion and source-follower combination.

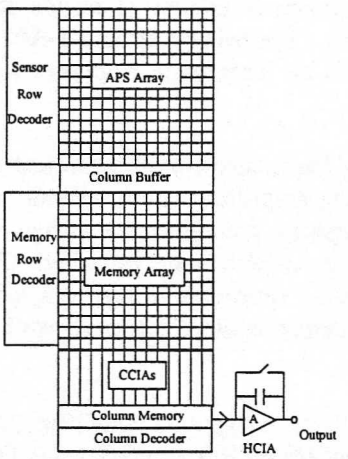

Figure 1 - Frame-transfer APS architecture

At the bottom of each column of pixels is an ac-coupled source-follower (henceforth called the buffer). When the pixel reset level is present on the column bus, the clamp switch MB1 is closed, clamping the input of the buffer to VCLP. The clamp switch is then opened and the pixel signal level is applied to the column bus. The buffer output is thus reduced by an amount proportional to the photosignal. Voltage offset from the buffer is suppressed by the column charge integration amplifier circuit, as described later.

Below the buffer is the array of memory cells. Each row of memory cells corresponds to a row of pixels in the APS array. The memory cell is a simple passive sample-and-hold switch and capacitor. When a row from the APS array is being read out, a corresponding row of memory cells is selected by R_Sel. The voltage from the buffer is sampled onto the memory cell capacitor C_M. When R_Sel is deactivated, the photosignals from the corresponding APS row are held on the row of memory cell capacitors.

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The frame-transfer operation consists of sequentially selecting rows in the CMOS APS, reading the pixels in the row, and writing the signals to the corresponding memory cell row. Total time to transfer a single row of pixel signals to a row of memory cells is approximately 2 μsec. (This is equivalent to a vertical transfer rate of 0.5 MHz in a frame-transfer CCD) Thus, to perform frame transfer on an array of 32 rows takes approximately 64 μsec. For an array with 512 rows, it would take 1 msec. Unlike a frame-transfer (FT) CCD, all rows need not be transferred, and they need not be selected sequentially. Faster transfer times are possible in future designs.

The frame-transfer operation allows the CMOS APS to capture images in "snapshot" fashion, thus eliminating flicker caused by indoor lighting, and motion-induced image skew. Unlike frame transfer in a CCD, no smear is introduced by the frame-transfer operation. The penalty for an FT-APS, like in a FT-CCD, is an increase in chip area for the frame memory.

Readout of the frame memory is performed using charge integration amplifiers. Each column has its own charge integration amplifier. The voltage output of the amplifier is sampled onto a capacitor. Charge from these column capacitors is read out using a global charge integration amplifier, as shown in Fig. 2.

The column charge integration amplifier (CCIA) consists of a standard folded-cascode op-amp [9] and switched capacitor (SC) network. The folded-cascode op-amp and SC network has the unique feature that it is designed to fit in the relatively narrow pitch of 24 μm in width. Additional circuitry is added to compensate not only for the op-amp input offset but also the signal mismatch error prestored in the memory cells. This suppresses fixed pattern noise (FPN) in the image sensor.

The charge on the column capacitors C_{MC} are sequentially selected for readout by the column decoder circuit. A given column is selected for readout by switch C_Sel. Prior to activating C_Sel, the horizontal charge integrating amplifier (HCIA) is reset by pulsing RSTO shorting its feedback capacitor C_O (1 pF). When C_Sel is activated for a particular column, the charge from the capacitor is converted to a voltage through the capacitance C_{CO}, resulting in a net voltage gain of 2 from C_{MC} (unity gain from C_M). The process continues until all columns that are desired to be read out have been selected. Column selection need not be sequential nor does it need to be scanned in a particular direction.

3. Binning Operation

CCDs have been operated in a binned mode almost since their inception. Charge from adjacent pixels in a column are summed in the horizontal register. Charge from adjacent columns are summed at the output node. The effective resolution of the CCD is decreased depending on how many pixels are summed in each direction. The signal-to-noise ratio (SNR) is increased by the square root of the number of pixels binned if the noise is dominated by shot noise and the SNR is increased linearly with the number of pixels binned if the noise is dominated by read noise. In a CCD, the binning operation is noiseless since summation takes place in the charge domain. This is a major advantage for CCDs.

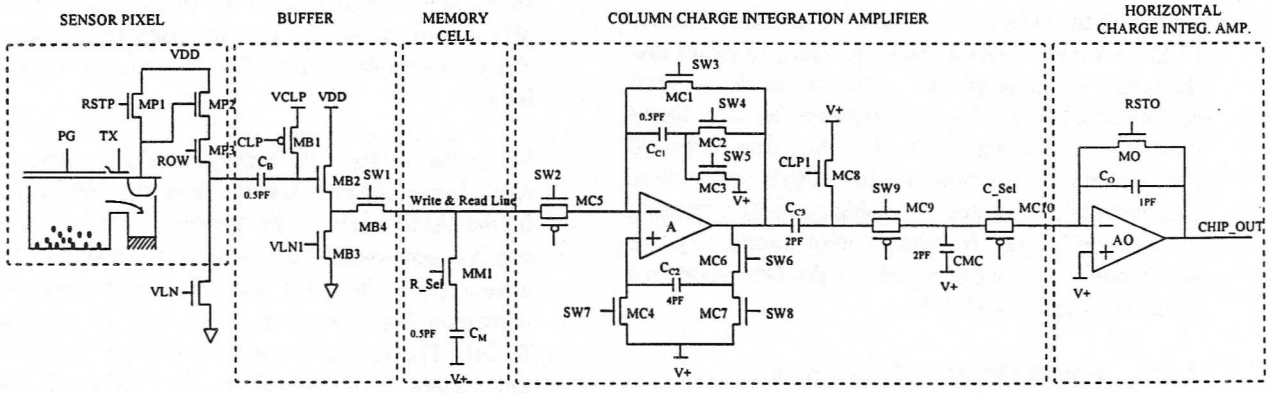

Figure 2 - Signal chain of the FT-APS readout.

An analogous operation can be performed for the FT-APS using the CCIA amplifiers and the HCIA. For vertical direction binning, charge from multiple memory cells can be summed using the CCIA by sequentially accessing the cells using R_Sel and integrating the charge on the feedback capacitor.

For the binning of pixels in adjacent columns, the HCIA is utilized. In this case, charge from multiple capacitors (C_{MC}) are summed in the HCIA by sequentially accessing those capacitors via C_Sel, without resetting the HCIA between selection of successive columns. Since the charge on the multiple capacitors represents a vertically binned signal, the output from the HCIA represents a 2-D binning of pixels of arbitrary kernel size. In the FT-APS, binning of pixels results in an improvement in SNR. However, because the binning process is not noiseless, the improvement in SNR is less than in the case of the CCD.

The resolution of the sensor is also modified by the binning process in the same way as for a CCD. It should be noted that the variable resolution offered by this approach is different from that previously reported for a multiresolution CMOS APS [10] because in the present case the signal grows as charge is binned. Summation is important for low light conditions where SNR can be improved at the expense of spatial resolution. In the previous work, the binned pixels are averaged, not summed. Averaging is important for common lighting conditions where summation would cause saturation of the sensor output.

4. Experimental Results.

A 32x32 element APS array and a 32x32 cell frame memory were implemented using the HP 1.2 micron single-poly, double metal process with linear capacitor option available through MOSIS. The APS array pixel size was 24 μm x 24 μm with a designed fill factor of 29% The sensor was measured to have a conversion gain of approximately 6 μV/e-.

The memory cell size was 24 μm x 28 μm with a memory cell capacitance C_M of 0.5 pF. Layout of the CCIA and SC network was 24 μm in width and 400 μm in length. Second level metal was used for routing in the frame memory and used for light shield in the pixel array periphery. Total chip size was 2.8 mm x 4.5 mm. Power dissipation was measured to be less than 1.6 mW at 400 kpixels/sec.

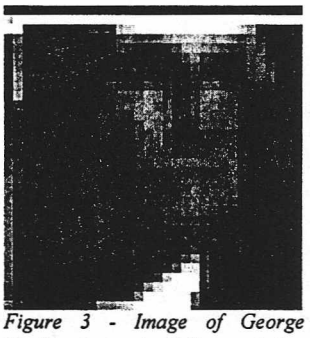

Figure 3 - Image of George Washington at full resolution taken at 100 kPixels/sec.

A full-resolution (32x 32) image captured from the frame-transfer APS is shown in Fig. 3. The image was captured at 100 kpixels/sec due to the maximum speed of the 16b ADC card used in the acquisition system. Due to a layout error, the first two rows and first two columns of the array were not functional. The sensor was successfully operated up to 400 frames per second for 400 kpixel output data rate. Higher operating speeds can be achieved with improvement to the HCIA. No blooming or smear was observed in the acquired images, though quantitative assessment of these parameters was not performed.

Fixed pattern noise in the sensor was quantitatively determined by uniformly illuminating the sensor array. With the pixel CDS circuit operational, but with the CCIA FPN suppression circuits deactivated by timing, the FPN in the output image was 40 mV p-p. Activation of the CCIA FPN circuit suppressed the FPN to below 15 mV p-p resulting in a 8.5 dB improvement. With a saturation level of 1 volt, the residual FPN is 1.5% sat or approximately 4 LSBs in an 8b system. Further improvement in FPN suppression is desired for the future.

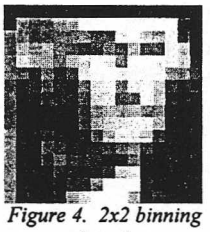

Figure 4. 2x2 binning of pixels.

A 2x2 pixel binning operation is demonstrated in Fig. 4. The apparent brightness of the image has increased as expected and SNR was improved. Improvement in output signal level with number of pinned pixels is plotted in Fig. 5.

Noise in the sensor was theoretically calculated to be 0.4 mV r.m.s. Experimentally, the noise was measured to be much higher at 3.1 mV r.m.s. It is felt at this time that residual test station noise has likely caused an anomalously high measured noise level but this hypothesis was not proven by the time of writing. Some improvement in SNR with binning was nevertheless observed, as shown in Fig. 6.

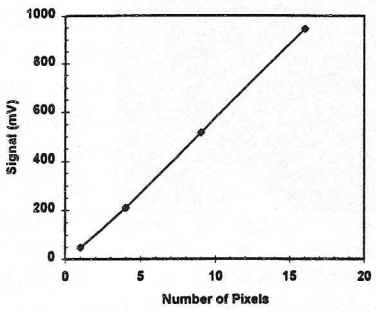

Figure 5 - Improvement in signal with number of pixels binned.

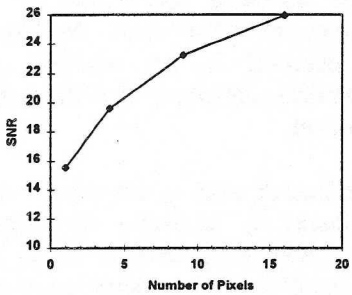

Figure 6. Improvement in SNR with number of pixels binned.

5. Conclusions

The first frame-transfer CMOS APS has been demonstrated. The sensor integrates an active pixel array with a passive memory cell array to permit frame-transfer operation. Charge integration amplifiers at the bottom of each column and a horizontal charge integration amplifier permit binning of pixel signals from arbitrary kernel sizes during the readout process. The results from the experimental sensor help illuminate options for future, larger frame-transfer APS devices with smart on-chip functions.

6. References

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