Design and Processing Aspects of a 50 Megapixel Full Frame CCD Image Sensor

Michael Farrier, Charles Smith
DALSA, INC.
605 McMurray Road, Waterloo, ON. Canada N2V 2E9
Tel.: 519-886-6000, Fax: 519-886-8023

William Pfister
CAI, a Division of RECON/OPTICAL, INC.
550 West Northwest Highway
Barrington, IL., USA 60010-3094
Tel: 847-381-2400, Fax: 847-381-1745

Abstract

A 5040 x 10080 element, sixteen tap, full frame CCD image sensor is in development for aerial reconnaissance applications. The array features 32 individually clocked vertical sectors to achieve image motion compensation and a frame rate of 2.5 frames per second. Aspects of the design include a 10 μm pixel pitch with metal strapping, > 140Ke- full well capacity, responsivity in the near infrared for twilight imaging, and horizontal register amplifier taps within a 10 μm horizontal register pitch. The process is a 6 in. wafer scale, three poly, n-buried channel process and requires photolithographic stitching of modular device segments. A profiled buried channel is used to maximize full well capacity and metal strapping layout is organized to reduce shorting due to random defects while maintaining low RC time constants. Considerations for yield, optical stitching artifacts, and device performance optimization will be discussed.

Introduction

High speed, high resolution image sensors have recently been developed for Aerial Reconnaissance applications[1]. Full frame CCD image sensors with 5040 x 5040 pixels at 12 μm x 12 μm pitch have been reported to achieve a frame rate of 2.5 frames per second using a metal strapped three phase polysilicon bus structure and eight output taps[2]. Near Infrared response and large dynamic range are critical requirements for this application.

Recon/Optical, Inc. (ROI) and DALSA, Inc. have pioneered the E-O framing reconnaissance technology with the invention of wafer scale FPA's with on-chip Forward Motion Compensation (FMC) in 1990[3]. The 4 and 25 megapixel sensors have seen operational deployment in a reconnaissance POD. The need for ever improving battlefield awareness through increased resolution and greater field of view sensors generates the requirement for an Ultra-High Resolution Digital EO Framing Camera program from NRL. We have answered this requirement for a 100 megapixel/second equivalent sensor with development of a 10k x 5k (50M) FPA. Figure 1 shows that at a 2.5 frame per second rate and wide cross-line-of-flight field of view, the 50M FMC array will cover the equivalent 100 megapixel resolution in less than 1 second.

Performance Goals and Device Architecture

Table 1 summarizes the performance goals and sensor format required for the 100 Megapixel equivalent demonstration. High data rate, Near IR sensitivity, and Wide Dynamic Range are critical concerns and drive the process technology. Reduction of single point defect density is also vital.

TABLE 1

Item	50 Megapixel Sensor	Comments
Array	5040(V) X 10,080(H)	Figure 2
Pixel Size	10 μm x 10 μm	30% shrink from previous
Number of output taps	16	2X previous design
Frame Rate	2.5 fps	127.1 Megapixels per second
Fill Factor	> 80%	
Nsat	>140 Ke-	
Vertical Clock Rate	> 500 KHz	Clocked Antiblooming
QE	> 40% at 750nm	> 20% at 900nm
Technology	3 poly, 3 phase, BCCD, 150 mm wafer, 5X optical stepper	Single metal, BCCD trench, Metal strapped

→ stitched device

Design Considerations

DALSA has reported on the development of 5K x 5K element, full frame CCD image sensors which achieve a frame rate of 2.5 frames per second, NIR response, and wide dynamic range[1, 2]. The previous design includes a 12 μm pixel, 16 independently clocked vertical sectors to achieve a clock rate gradient for image motion compensation(4), and 8 amplifier taps within the three phase HCCD register. The process is based on scanning lithography using 100 mm substrates.

The 5K x 10K sensor design and process must maintain or better the performance feature of the 5K x 5K sensor. It is necessary to establish a three polysilicon, BCCD process, with strapping, low dark current, and acceptable yield on 150mm substrates. Currently available CCD processes on 150mm substrates utilize vertical antiblooming p-well structures which have poor NIR response. To achieve adequate NIR response it is necessary to eliminate the VAB p-well on N-type substrate and convert to a P-epi substrate. Buried channel profiles(figure 3), thresholds, and various operating parameters are affected.

For yield considerations it was necessary to shrink the pixel to a 10μm pitch while maintaining responsivity and full well with a 30% smaller pixel area. Full well is maintained by increasing the size of the profiled channel by 80% from the current 3 μm to 5.4 μm wide and by reducing the channel stop by 300% from 4 μm to 1 μm. The calculated net full well capacity is 15% to 25% greater than that of the 12 μm pixel design. Fill factor for the 10 μm pixel design is reduced by 17% which is determined by the final width of the metal strap covering the channel stops. The reduction in pixel quantum efficiency is mitigated by an increase in on-chip amplifier gain. A three stage source follower amplifier with reduced sensor node and first stage SF gate capacitance improves the charge to voltage gain from 1.5 μV/el. to 3.0 μV/el.

For reduced metal shorting, active metal busses are grouped in clusters of like phase. Non-active metal busses are interspersed between active metal buses. Spacing of bus clusters

is calculated to produce tolerable propagation delay on vertical clocks while still reducing the probability of metal bridging shorts[4]. This technique was previously developed and successfully used on other DALSA products.

Yield Considerations

The sectored 5K x 5K sensor is an excellent vehicle for studying the yield vs. area for the process. Yield studies indicate that the yield of contiguous sectors follows the classical exponential $Y = e^{-AD}$ for device area up to approximately 80% of the 16 sector device. As the device area increases to 16 sectors, the yield value fluctuates dramatically and the exponential yield model no longer applies.

Through extensive defect studies, it has been possible to identify, and in some cases, circumvent, defects which create vertical clock shorting. The majority of shorting failures are medium to high resistance shorts of vertical clocks suggesting that the mechanism is poly inclusions which rupture the interpoly dielectric at poly overlaps. Random mask/etch voids in the contact/Via dielectric layers and stress induced breakdowns of intermetal dielectric are also sources of shorting. Second metal shorting is avoided, in the 50 Megapixel design by using a single metal layer for bussing.

Generally, defects which would create imaging artifacts also create shorts, hence, imaging defects are generally low in density for non-shorted devices. Imaging artifacts, created by the optical stitching pattern of the 5X stepper system, are known to generate fixed pattern PRNU. Stitching seams mostly can be buried at sector boundaries. Metal and channel stop patterns must be crafted such that mis-alignments do not create excessive PRNU.

Conclusion

The construction of high frame rate wafer scale CCD image sensors, with performance features specific to aerial reconnaissance systems, presents unique challenges for CCD image sensor technology. Using processes with reduced defect densities and novel, short resistant, layout practices, it is possible to build high speed, full spectrum, multi-tap, full frame CCD image sensors containing more than 50 million picture elements, operating at greater than 2.5 frames per second.

Acknowledgments

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References

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207 pin ceramic pkg. 3μV/e⁻ 7.5 W @ 2.5 fps

Figure 1, Schematic of High Resolution Frame Imaging Application

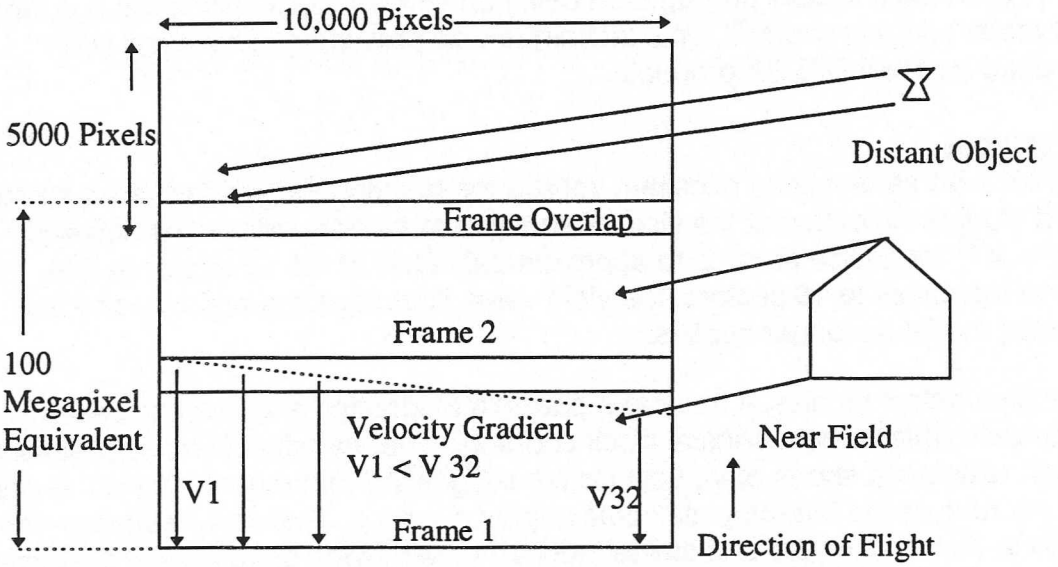

Figure 2, 5040 x 10,080 Element Full Frame Sensor Block Diagram

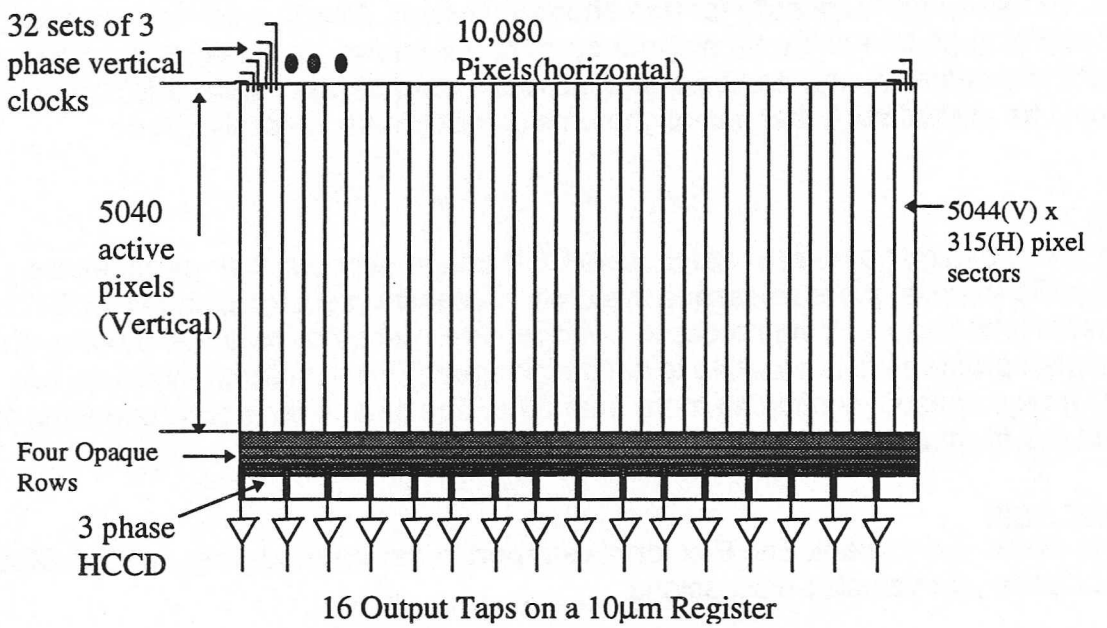

Figure 3, Pixel Cross-Section