Technology and Performance of VGA FT-Imagers with Double and Single Layer Membrane Poly-Si Gates

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Abstract

For the first time a single layer membrane poly-Si gate technology is used to fabricate FT-VGA imagers and could be used to fabricate imagers with pixel sizes of 3 x 3 μm^2 and larger in conventional design rules of 0.5 μm. The separation technology of the gates is based on the tapered contact hole technology.

Introduction

The strong market demand for Digital Still Cameras and cameras for PC-applications is obvious. Consequently the need for VGA-imagers (640 x 480 pixels) and QGA-imagers (1280 x 960 pixels) is increasing as well. At the same time the optical format has to be shrunk from 1/3" [1] to 1/4" [2] to 1/5" [3] and even to 1/8" [4]. Forced by these developments we recently proposed a new technology to achieve very small pixels of **2.4 x 2.4** μm^2, 3 x 3 μm^2, 4 x 4 μm^2 and 5.1 x 5.1 μm^2 for VGA FT-imagers with an optical format of **1/8"**, 1/7", 1/5" and 1/4" respectively [4]. With conventional design rules of 0.5 μm, double membrane poly-Si gates, 0.2 μm tapered contact holes and sunken tungsten shunt wiring [5] were implemented in these imagers.
In this paper we compare the sensitivity of FT-VGA imagers made in this technology that have pixel sizes of 5.1 x 5.1 μm^2, run in 3 or 4-phase clocking mode, and have different kinds of microlenses. Although the results are in favour for the 3-phase operating devices, these sensors are less valuable because of pixel non-uniformity when two poly-Si layers are used to define the gates.
To solve this problem we propose for the first time **a single layer membrane poly-Si gate** technology, which always results in the same pixel construction irrespective of the number of phases. The technology is described and special attention is paid to the separation of the transfer gates.
Especially in IT-imagers several studies have been carried out to use single (thick) poly-Si gate structures for simplifying the technology with a high degree of planarisation, and for obtaining low power consumption [6,7]. They all suffer from potential barriers at the interelectrode gaps with charge transfer degradation problems, so an additional inter-electrode implantation of boron is needed. The new proposed separation technology of the transfer gates is based on the 0.2 μm tapered contact hole technology [4], so the inter-electrode gap is 0.2-0.25 μm as well and consequently additional inter-electrode implants are unnecessary.

Tapered contact holes (vias)

This technological step is of crucial importance for the realization of small pixels with dimensions of $\leq$ 4 x 4 μm^2 with 0.5 μm design rules, to connect the shunt wiring to the membrane gates (smallest gate length is 0.45 μm). In a relatively thick isolation layer (e.g. 1 μm) holes of 1 μm diameter with a depth of 0.5 μm are etched above those regions where we want to make very small contacts. A TEOS layer of 0.5 μm is then grown over the structure, followed by maskless anisotropical etch back until the desired layers are reached, resulting in nicely tapered contact holes with a bottom diameter of $\leq$ 0.25 μm. A SEM picture of a tapered via, filled with poly-Si is shown in Fig.1. In Fig.2 the supporting poly-Si pattern for the tungsten shunt wiring, and for the filling of the tapered contact holes at the same time, is shown after deprocessing (by etching away all the reachable oxide).

Gap-less microlenses

Both the use of membrane poly-Si gates of 60 nm, as well as the in-situ formation of microlens-shaped wrinkles above the tungsten shunt wiring, results in high sensitivity of our VGA and QGA imagers [4], see Fig.1.
More sensitivity is obtained by using optimized microlenses. These lenses are made of heat-resisting material, and can easily be realized by transferring convex resist lenses into a hard substrate material by anisotropic reactive ion etching. The selectivity between photo-resist and the heat-resisting material amounts to 1 : 1. With this procedure a relatively large distance (gap) of about 0.7 μm between the microlenses is inevitable.
An optimal sensitivity is obtained by eliminating the gaps completely, simply by depositing an extra 1 μm layer of the same microlens material. See Fig.3.

Sensitivity measurements

FT-VGA imagers with pixel sizes of 5.1 x 5.1 μm^2 have been made in the double membrane poly-Si gate technology, with both 3 and 4-phase clocking pulses , and with microlenses and gap-less microlenses. Sensitivity measurements on imagers with gap-less microlenses are shown in Fig. 4, and the effective sensitivity improvements are summarized in Table I.
In spite of the lower sensitivity it it is advantageous to do the integration of the image with 2 blocking gates when 4-phase clocking pulses are used. In comparison with integration under 3 gates, the charge storage is larger with the same electrical driving conditions of the imager. The barrier height of one blocking gate is too low for small pixels with short gate length.
The results clearly support the application of imagers in a 3-phase vertical clocking mode.
However, 3-phase operating FT-imagers suffer from pixel non-uniformity, when 2 poly-Si layers are used for the realization of the gates. One pixel will contain two gates in poly-1, the other two gates in poly-2. Differences between the poly-Si layers will appear as a higher FPN in images.

Single layer membrane poly-Si gate technolgy

To solve this pixel non-uniformity problem, the single membrane poly-Si gate technology has been developed, resulting in identical transfer gates with equal gate-dielectric layers for every clocking system. This technology is based on the tapered hole technology as mentioned before.
After deposition and doping of the membrane poly-Si layer (50-60 nm) a silicon nitride layer (40 nm) and a relatively thick oxide layer (>0.5 μm) are deposited. Then grooves (0.5 μm wide) are etched using conventional lithography (0.5 μm design rules) to half the thickness of the deposited oxide layer. The pitch is equal to the gate length. Again an oxide layer is deposited (0.25 μm), followed by an etch back until the membrane poly-Si has been reached. Now the deposited oxide can be stripped. The spacing in the nitride pattern is 0.2 μm and can be reproducably made. To continue defining the gate structure there are 2 options, see Fig.5 :
a) separate the membrane layer into gates by anisotropic etching and do a wet sidewall oxidation
b) separate the membrane layer into gates by a LOCOS step.
In both cases we make use of an interesting phenomena related to the Kooi effect [8], that causes retarded oxidation of very thin poly-Si layers encapsulated by nitride. The gap between the gates can be controlled by the retardation of the oxidation. Oxidation is necessary for yield reasons to eliminate shorts causing poly-Si residues in the gaps. In Table II experimental results are shown of oxide thicknesses on Si, poly-Si, thick poly-Si sidewalls and membrane poly-Si sidewalls. The retardation is obvious for the case of membrane poly-Si sidewalls. The proof that Kooi's model plays a dominant role to explain the effect, is demonstrated by a dry oxidation of the same membrane poly-Si sidewall. 80 nm and 140 nm membrane poly-Si sidewall oxide thickness was measured respectively for wet and dry oxidation, although in both cases a 100 nm oxide thickness had been measured on mono-Si.
An attractive option for the separation technology would be option a), because of the possibility of narrow etch gaps with a short sidewall oxidation. It fails however, because the sidewall oxidation should be able to oxidize away any poly-Si shorts with membrane thickness. That means the effective gap-width will exceed 0.3 μm (see Table II), and degradation of charge transfer efficiency may start when no extra inter-electrode boron implant is done. Option b) is the best solution, because the effective separation gap is only 0.2 μm, and additional inter-electrode implants are unnecessary. See Fig. 5b. Optimization of LOCOS time will result in even smaller effective gaps. Option b) provides also relatively flat surfaces.
3-Phase VGA-imagers made with single membrane poly-Si gates retained all properties of our double membrane poly-Si gate VGA imagers [4], except for the sensitivity and the pixel uniformity. Both have been improved. As shown in Fig. 6 the sensitivity improvement is especially in the red.

Conclusions

Sensitivity measurements show optimal results for VGA imagers made in double membrane poly-Si gate technology, operating with 3-phase clocking pulses. With **gap-less microlenses** almost 60% Q.E. has been achieved. Due to pixel non-uniformity in such 3-phase clocking systems, however, a **single layer membrane poly-Si gate technology** has been developed to obtain identical pixels for all kinds of clocking systems. The separation technology of the gates is based on the **tapered contact hole technology**, combined with a LOCOS technology to obtain narrow gaps between the gates of 0.2 μm. This technology does not require an extra inter-gate implantation.

References:
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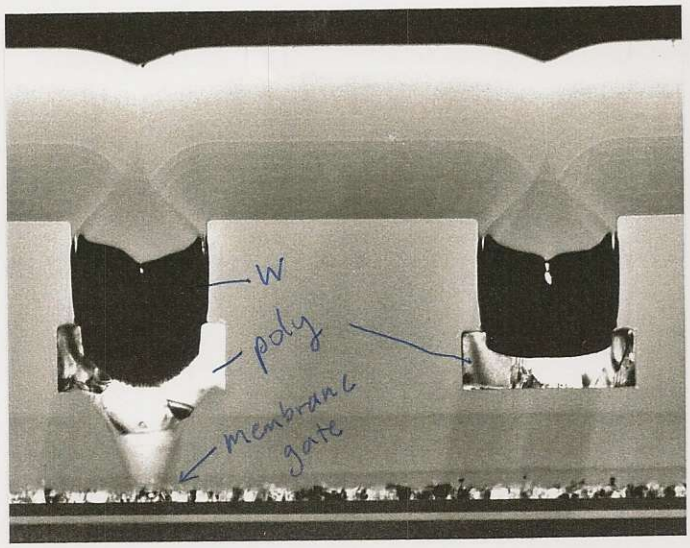


Fig. 1. TEM cross-section of a tapered hole filled with poly-Si contacting a membrane poly-Si gate, and of tungsten shunt wiring and in-situ microlenses.

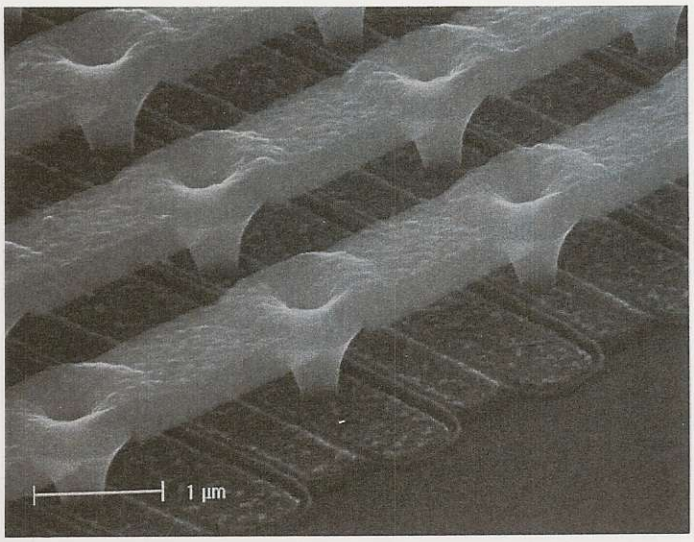


Fig. 2. Perspective view of poly-Si pattern for supporting tungsten shunt wiring and contacting membrane poly-Si gates, after deprocessing.

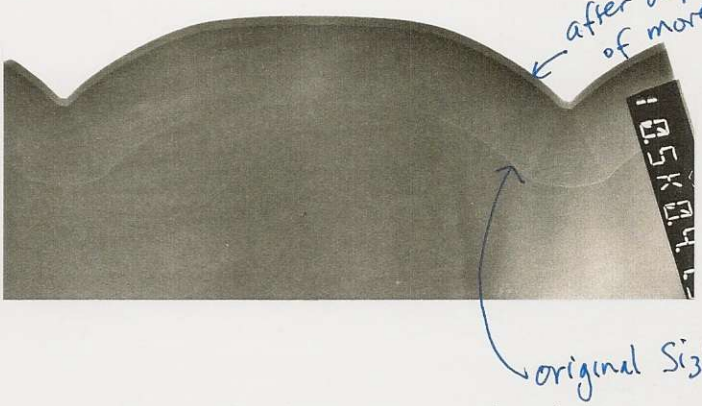


Fig. 3. Gap-less microlenses consisting of hard microlenses covered with an extra layer of the same material.

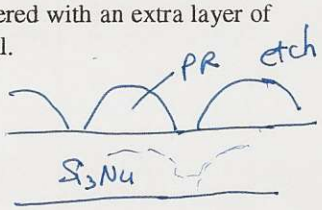
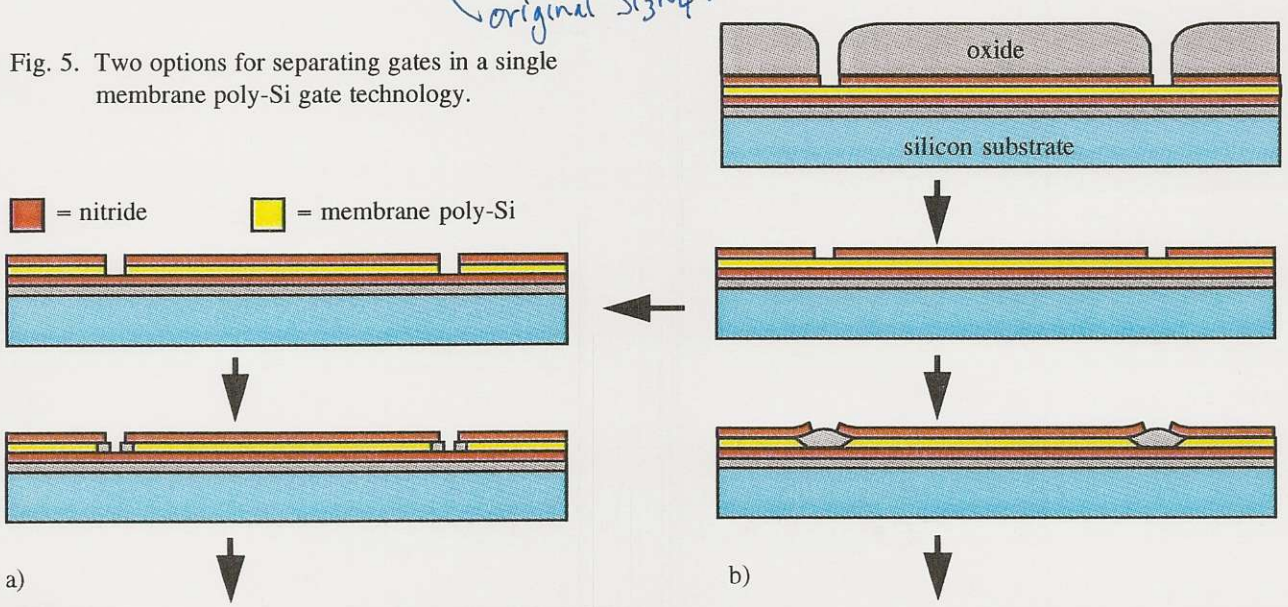
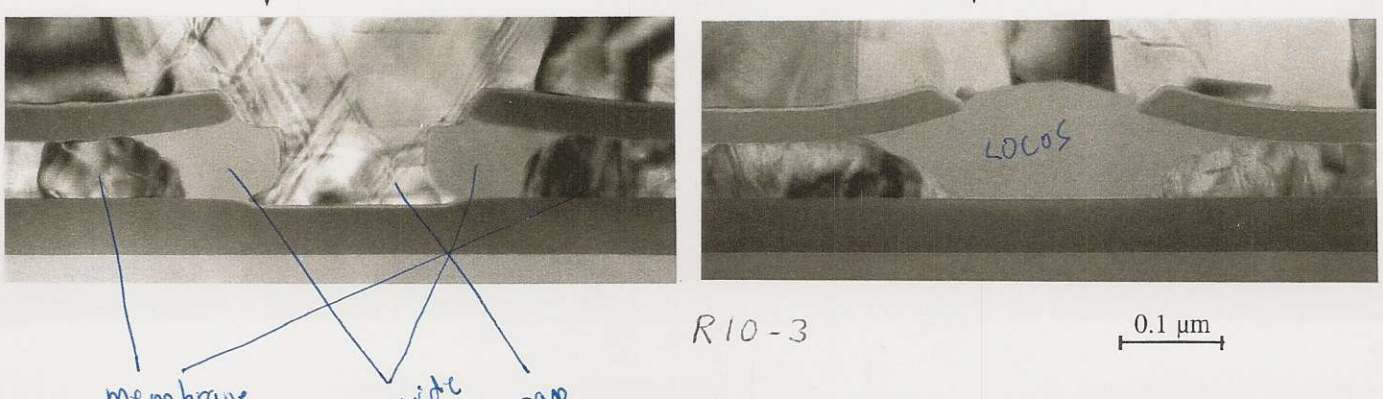


Fig. 5. Two options for separating gates in a single membrane poly-Si gate technology.





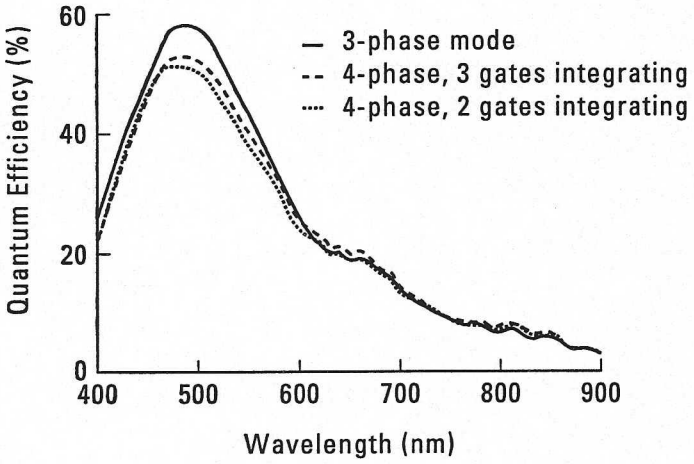


Fig. 4: Quantum efficiencies of VGA sensors with gap-less microlenses and pixel sizes of 5.1 x 5.1 μm^2, operating in different modes

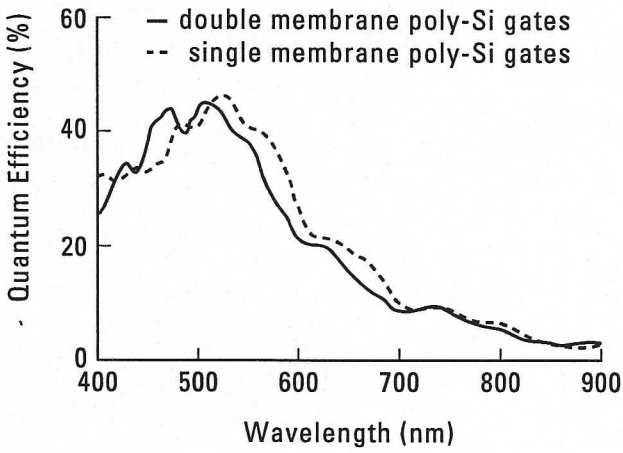


Fig. 6: Quantum efficiencies of VGA sensors with pixel sizes of 5.1 x 5.1 μm^2

Table I

Effective Quantum Efficiëncy improvement (%) (reference is a 4-phase standard pixel with in-situ microlenses)	4-phase 2 gates integr.	4-phase 3 gates integr.	3-phase
5.1 x 5.1 μm^2 pixel with in-situ microlenses	-	8.0	9.2
5.1 x 5.1 μm^2 pixel with microlenses	12.7	22.6	24.8
5.1 x 5.1 μm^2 pixel with gap-less microlenses	27.1	33.6	42.0

Table II

OXIDATION 1000°C

Option	Oxidation	Time (min)	Oxide thickness (nm) on mono-Si	on poly-Si	Sidewall oxidized thick poly-Si	Sidewall oxidized membrane poly-Si	Gap width (nm)
a	wet	8.5	100	170	150	80	290
a	wet	16	150			100	330
a	wet	24	200	280	230	110	360
b	wet	24	200	280	230		200
a	dry	100	100			140	500