A bipolar imager with bipolar field memory

Mahito Shinohara , Shigetoshi Sugawa, Yoshio Nakamura, and Tadahiro Ohmi*

Device Development Center, Canon Inc.
6770 Tamura, Hiratuta-shi,Kanagawa 254, Japan

* Department of Electronic, Faculty of Engineering, Tohoku University
Sendai 980, Japan

Abstract

A 100H×70V pixel bipolar imager designed to detect an image signal of near-infrared LED rays is reported. The imager, fabricated using 2 μ m Bi-CMOS process, consists of bipolar sensor cells, bipolar memory cells, and signal transfer circuits. The sensor cell is 16.6 μ m×16.6 μ m in size and its aperture ratio is 67%. The device, utilizing performance specific to bipolar APS, amplifies signal charges and cancels noises to hold a high S/N ratio signal in the memory. It also has several functions such as cancellation of external light signal and two readout modes. Equipped with CMOS peripheral circuits, the chip is 3.66mm×3.7mm in size.

Ⅰ.Introduction

Up to now, several types of active pixel sensors(APS) were proposed[1]-[6]. APS's feature low power consumption, X-Y address-ability and non-destructive readout in common, but require efforts to reduce their considerable noises. In addition to noise suppression, it is important to open up application methods that can make the best use of the APS characteristics.

There is need for the imager that detects an image of LED rays and outputs the signal to an external processor. Field memory is necessary to hold the image signal during image process. High sensitivity to near-infrared rays, low noise, and immunity to dark current in the hold period is desired. Functions such as cancellation of external light signal and low resolution readout followed by main readout of selected part could be helpful to exact and rapid image process.

The imager was devised to give sufficient properties and functions by utilizing bipolar APS called BASIS[5]. The chip concept is illustrated in Fig.1, which includes a logic circuit and an analog circuit. As these peripheral circuits for controlling the chip operation are subsidiary, this paper centers on and describes essential structure and performance as the image detector.

Ⅱ. Basic Structure and Operations

The basic circuit configuration is shown in Fig.2. The sensor and memory cells are both typical BASIS pixels. BASIS, which stores signal carriers in its base region, is characterized by its reset and readout operations. Just after charging its base with hole carriers through its pMOS transistor, the base is reset by emitter current. The base potential after the reset is determined by its emitter potential fixed then. The emitter reset potential of sensor cells is VC, or standard potential of this imager. The memory cell, on the other hand, uses the reset as a signal writing operation, in which

its emitter is set at the potential that the signal transfer circuit gives. Different from other general APS pixel outputting its signal with load current, BASIS pixel performs readout using load capacitor: base signal charges multiplied by current gain are distributed to the capacitance connecting to the emitter. BASIS, therefore, suffers from partial destruction in the readout. Random noises that BASIS generates are reset noise represented as $(kT/CB)^{1/2}$ with voltage unit and readout noise resulting from fluctuation of the number of holes flowing from the pixel base. CB is the base capacitance.

The transfer circuit consisting of a Darlington-connection emitter follower and a capacitance connecting to its input part plays a role in providing the memory cell with the output potential. The circuit takes potential difference between two sequent signals by using the capacitance coupling.

Ⅲ.Properties and Functions

Sensitivity to near-infrared rays depends on the vertical reach of carrier collection in a sensor cell. BASIS based on vertical npn structure proves advantageous in this regard. The imager, positioning the collector at 10 μ m depth, presents 37% quantum efficiency for 880 nm wavelength rays.

The noises can be reduced by noise canceling operation mode, as shown in Fig.3. First, sensor cell noise generating at sensor reset is transferred to the memory cell. After signal accumulation in the sensor cell, difference between sensor output and memory output is written in the memory cell. In this mode, random noise of the sensor cell, fixed pattern noises(FPN) of the sensor cell, the transfer circuit, and the memory cell are canceled. Calculation reveals that the remaining random noise is caused mainly by reset noise of the memory cell; readout noise is much smaller owing to high current gain. Therefore, much greater memory cell capacitance could reduce the random noise further. The memory cell capacitance designed to be about four times greater than the sensor cell capacitance as shown in Table1. increases durability of memory signal to dark current noise, because signal charge is amplified at memory writing by a factor of the cell capacitance ratio.

The external light signal that would distort the real image can be also canceled: difference between external light plus LED rays signal and only external light signal is written to the memory. This operation increases random noise due to sensor resets performed twice, as shown in Fig.3.

The other functional operation is block readout, which gives averaged signal of several memory cells by using CT matrix shown in Fig.4. This readout is used to select a part necessary to be processed and is followed by a main partial readout using X-Y address-ability. Such a low resolution and repeated readouts to cut down unnecessary information are specific to APS devices and were already proposed[7]. This method is considered to be appropriate particularly for APS field memory that is free of incident light and of readout destruction.

Ⅳ. Conclusion

A 100H×70V pixel bipolar imager has been devised. Introduction of bipolar field memory and signal transfer circuit brings out characteristics of bipolar APS. The imager can reduce FPN and random noise. High sensitivity to near-infrared rays and durability to dark current noise are achieved. The detector functions to cancel external light signal. Low resolution readout and partial readout from field memory are effective to shorten image process time. The method discussed here might bring about one step of progress in APS devices.

Reference

[1]K.Matsumoto, et al., "A new MOS phototransistor operating in a non-destructive readout mode," Jpn J. Appl. Physics, vol. 24(5) pp.L323-L325, 1985.

[2]A.Yusa, J.Nishizawa, M.Imai, H. Yamada, J.Nakamura, T.Mizoguchi, Y.Ohta and M.Takayama, "SIT Image Sensor : Design Consideration and Characteristics," IEEE Trans., vol.ED-33(6), pp. 735-742, 1986.

[3]J.Hynecek, "A new device architectures suitable for high resolution and high performance image sensors," IEEE Trans. Electron Devices, vol. ED-35(5) pp.646-652, 1988.

[4]F.Andoh, et al., "A 250,000-Pixel Image Sensor with FET Amplification at Each Pixel for High-Speed Television Cameras," ISSCC Digest of Technical Papers, pp.212-213, Feb.,1990.

[5]N.Tanaka, et al., "A 310K pixel bipolar imager (BASIS)," IEEE Trans. Electron Devices, vol. 37, pp.964-971, April 1990.

[6]S.K.Mendis, S.E.Kemeny and E.R.Fossum, "A 128×128 CMOS Active Pixel Image Sensor for Highly Integrated Imaging Systems," IEDM Tech. Digest, pp.583-586, 1993.

[7]S.Kemeny, B.Pain, R.Panicacci, L.Matthies, and E.Fossum, "CMOS Active Pixel Image Sensor Array with Programmable Multiresolution Readout," 1995 IEEE Workshop on CCD and AID.

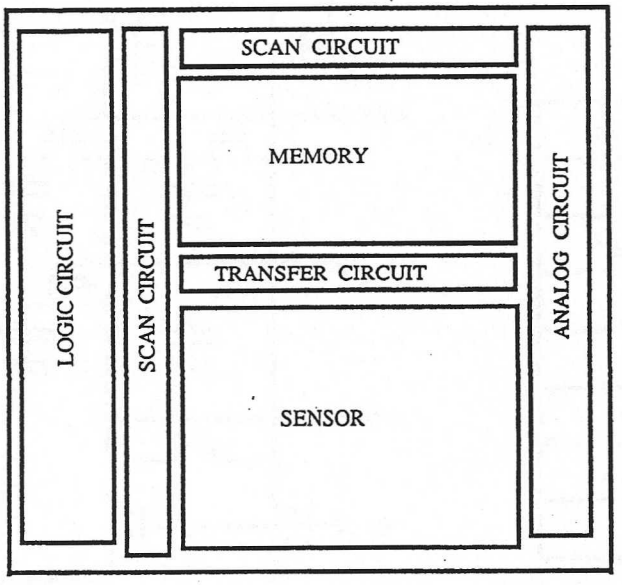

Fig.1 Chip Structure

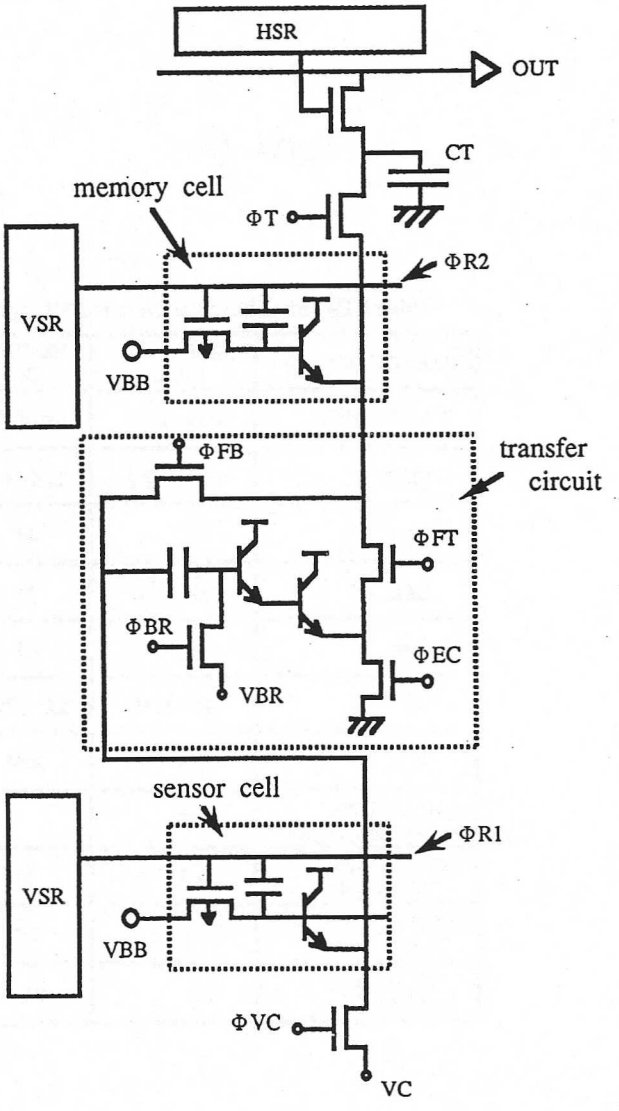

Fig.2 Basic Circuit Configuration

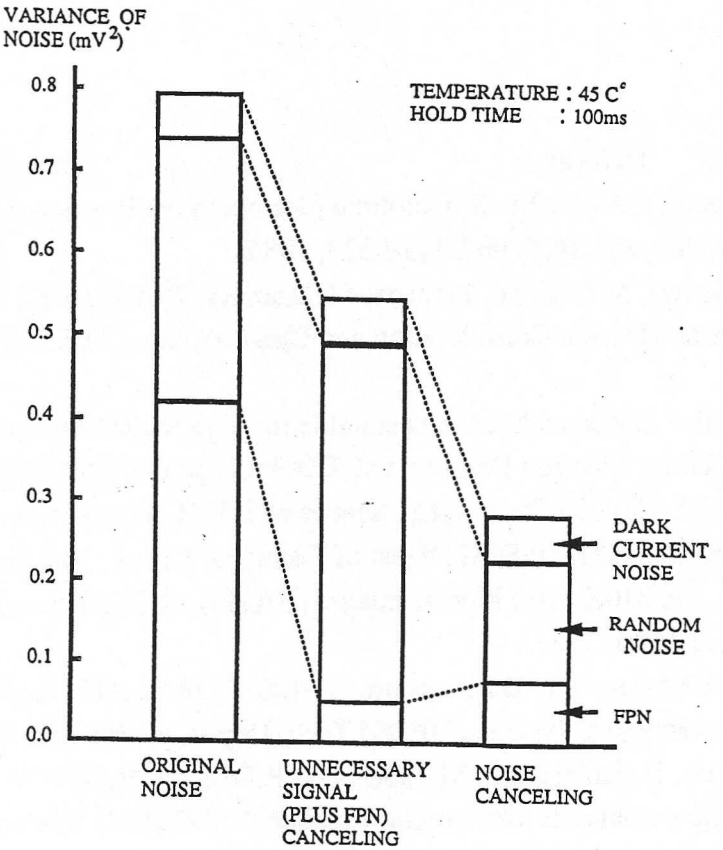

Fig.3 Noise Component

Table1.Device Characteristics for 5V Operation

CHARACTERISTICS	SENSOR CELL	MEMORY CELL	UNIT
THE NUMBER	100 × 70	100 × 70	
SIZE	16.6 × 16.6	16.6 × 14.3	μm^2
COX	10	80	fF
CBC	12	20	fF
CBE	6.1	6.1	fF
CE	0.7 (CV)	2.0 (CV+CT)	pF
h_{FE}	2000	2000	
SENSITIVITY (880nm wave length)	20		$V/\mu W\,cm^{-2}s$
SATURATION VOLTAGE	1.3	2.1	V
DESTRUCTION RATE	2%	1%	$READOUT^{-1}$
DARK OUTPUT VOLTAGE	120	90	mV

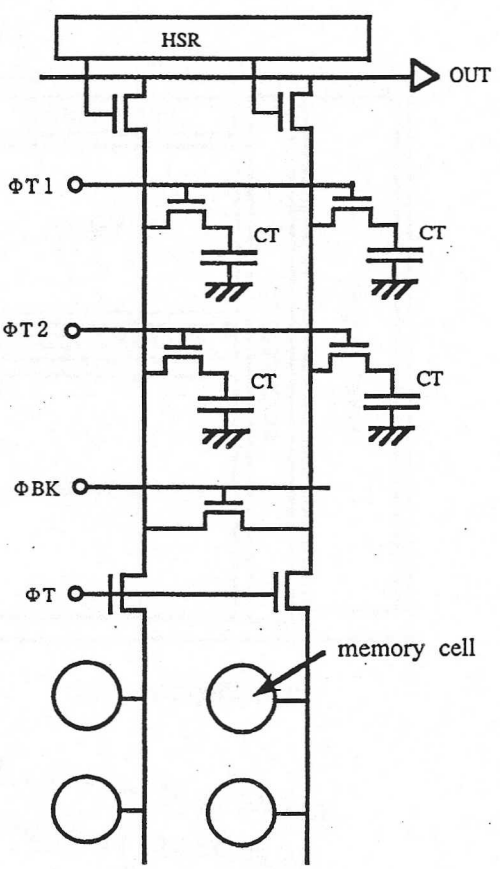

Fig.4 Circuit for Signal Mix