Fast CMOS Imaging with High Dynamic Range

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Abstract— **In this communication we report on our experience in 2-D imaging based on standard CMOS technology that features high speed, high dynamic range, and random pixel access. We have designed and integrated a 128×128 pixel imager with hexagonal structure in a standard 1 μm CMOS process. The pixels measure $29.1\mu\text{m} \times 25.2\mu\text{m}$ and have a fill factor of 40 %. The optical dynamic range is 140dB with a signal-to-noise ratio of 56dB.**

Keywords— **Vision chips, APS, CMOS-imager**

I. Introduction

CMOS-BASED photosensors are gaining more and more foothold in imaging applications [1], [3], [6]. Although they enable image acquisition similarly as CCD imagers do, there are some significant differences. Among others the CMOS approach provides the choice between linear and logarithmic pixel readout characteristics, yields random pixel access, and enables realisation of active pixel sensors. We have combined these three features and implemented a fast 2-D CMOS imager which exhibits $3\,dB$ pixel cut-off frequency of $1\,MHz$, $0\,dB$ pixel frequency well above $3\,MHz$, and a dynamic range of $140\,dB$.

The intended application is portable imaging systems. These require low power consumption due to battery operation and a high dynamic range, since in natural scenes the light intensity can vary up to 7 decades.

We have also implemented the sensor array on a hexagonal sampling grid which provides a good circular symmetry.

II. Design Considerations

While the linear pixel readout of CMOS imagers (e.g. using photocurrent integration) is capable of reproducing high contrast of an original image, it poses problems when a high illumination range is required. For such applications the logarithmic pixel readout is preferable. In our case we have used the circuit shown in Fig. 1. The pixel contains a photodiode formed between an n^+-diffusion and p-substrate and a pixel amplifier Q_2 and Q_3 with a feedback MOS-transistor Q_1 operating in weak inversion. As the feedback maintains an almost constant voltage accross the photodiode it renders the capacitance of the photodiode D ineffective and the circuit exhibits a very high frequency bandwidth, even at dark currents.

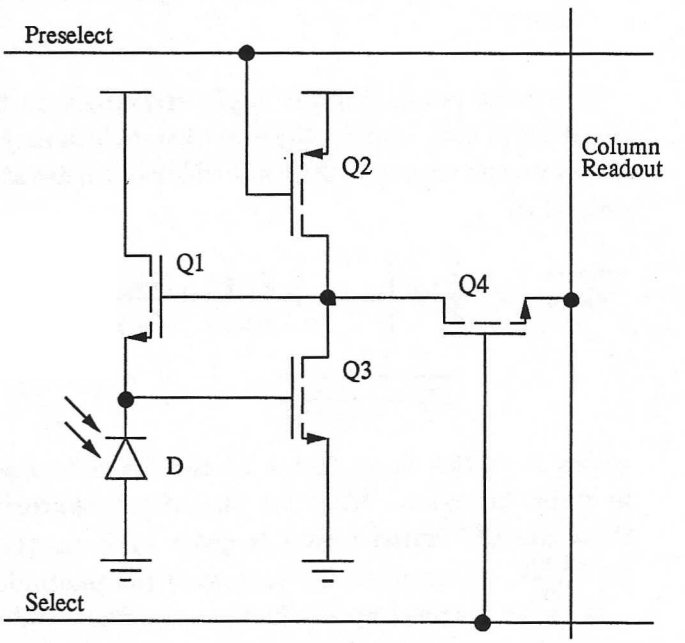

Fig. 1. Schematic of the pixel cell

Thus for $g_{m,Q3} \gg g_{m,Q1}$, $R_L = r_{ds,Q2} \parallel r_{ds,Q3} \parallel r_{ds,Q4}$, $g_{m,Q3} \cdot R_L \gg 1$, and $C_F = C_{gs,Q1} + C_{gd,Q3}$, the dominant pole can be approximated as

$$|p_1| \approx \frac{g_{m,Q1}}{C_F + \frac{C_D}{g_{m,Q3} R_L}} , \qquad (1)$$

where C_D is the capacitance of the photodiode.

The result is that the photodiode operates at high speed also at light-to-dark transitions. It is capable of detecting light modulation frequencies above $3\,MHz$ (see Fig. 2). The price paid is higher fixed-pattern noise as the mismatch contribution of both types of

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devices Q_1 and Q_3 to spatial noise is not reduced. Only the noise contribution due to Q_2 is reduced by the ratio $g_{m,Q3}/g_{m,Q2}$.

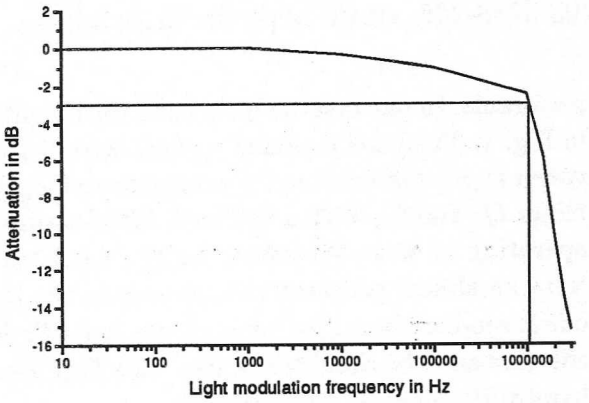

Fig. 2. Normalized sensor output vs. light modulation frequency

The same considerations apply essentially to temporal noise. Considering the noise bandwidth as $f_N = |p_1|/4$ we can estimate the total wideband noise at the output as

$$\overline{v_{out,n}^2} \simeq \frac{2}{3} kT \left[n + 1 + \frac{g_{m,Q1}}{g_{m,Q3}} + \frac{g_{m,Q1}}{g_{m,Q3}} \cdot \frac{g_{m,Q2}}{g_{m,Q3}} \right] \cdot \frac{1}{C_F + \frac{C_D}{g_{m,Q3} R_L}}, \quad (2)$$

where n is the slope factor of the MOS transistor in weak inversion. Also, for the above approximations the DC transfer gain is given by $1/g_{m,Q1}$, i.e. by $\frac{n\,kT/q}{I_D}$, where I_D is the current of the photodiode.

In order to speed up the image acquisition and still maintain low power dissipation, we have decided to use a preselection circuitry that activates preselected rows in advance.

This departs from the usual approaches where the rows are activated during the actual readout. Hence the timing and control circuitry of the realized imager contains not only row and column decoder and drivers, but also a user programmable row preselect circuit. The column select operation is carried out by activating the device Q_4 of the pixel which enable signal readout, while preselect activates the device Q_2. Thus the pixel circuit can settle down prior to the readout action. This measure reduces the row access time while maintaining a low power consumption, because only a few rows are active.

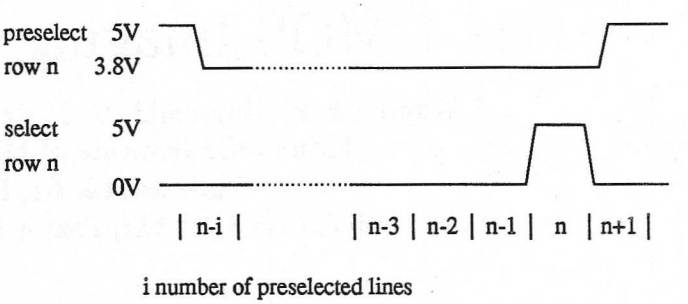

Fig. 3. Timing diagram of the preselect operation

III. Chip Description

We have designed an imaging sensor with 128×128 pixels in standard $1\,\mu m$ double-metal CMOS technology featuring n-well and p-substrate. The architecture of the chip is depicted in Fig. 4. A 1-to-128 decoder is used for the row selection of the hexagonal sampled sensor array containing 128×128 pixels. The preselect circuitry consists of a 1-to-128 decoder that addresses the latches used in each row. Depending on the state of the latches the current sources Q_2 in the pixels of the corresponding rows are activated. The readout electronics uses a tree structure. In the first stage four groups each consisting of 32 wires are multiplexed down to four. The remaining four interconnects are then multiplexed down to one output. Therefore, the required throughput at the output node of the column amplifier is reduced.

The pixel size is $29.1 \times 25.2\,\mu m^2$ with a fill factor of 40 % and the chip size is $24.6\,mm^2$. The measured dynamic range is $140\,dB$ (see Fig. 5) at $5\,V$ power supply voltage. The maximum pixel clock frequency is greater than $4\,MHz$ and the frame rate exceeds 150 frames/s at all irradiance levels. The sensor gain is $86\,mV$ / irradiance decade and the smallest detectable irradiance is below $10^{-3} W/m^2$ (see Fig. 5). Fig. 7 shows several test images taken in our laboratory.

The dependence of column settling time for different irradiance levels without preselection operation is shown in Fig. 6. For levels above $1 W/m^2$ the settling time is better than $5\,\mu sec$, but at $2\,mW/m^2$ it decreases down to $2.5\,msec$, although still allowing $400\,Hz$ pixel rate. When the preselection circuit is active, the column settling is always better than $6\,\mu sec$, independent of irradiance.

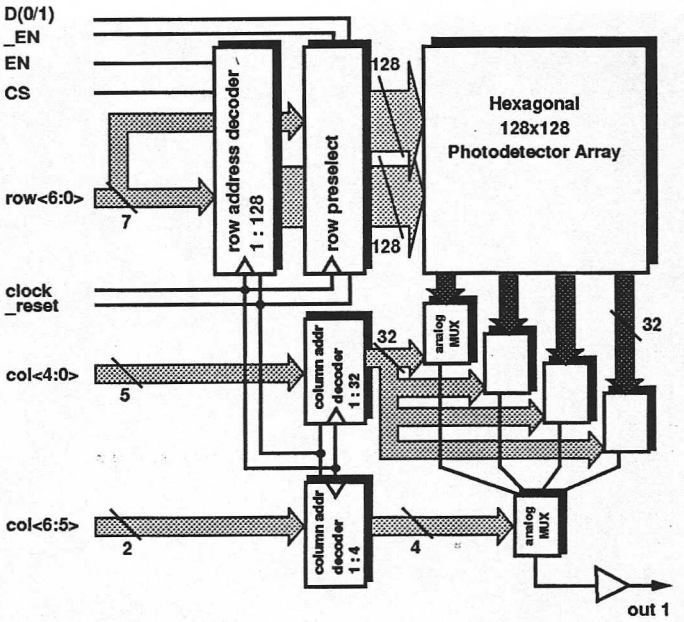

Fig. 4. Chip architecture

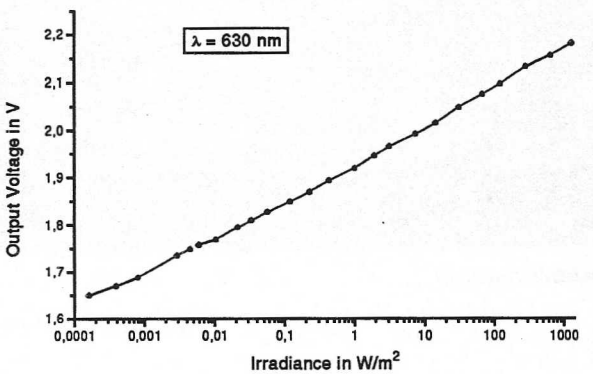

Fig. 5. Transfer characteristic of the pixel cell

IV. Technical data

Number of pixels	128 × 128
Pixel pitch	29.1 μm × 25.2 μm
Chip area	24.6 mm^2 in 1 μm CMOS
Power consumption	6 $mW/preselected\ row$
Sensor dynamic range	10^7
Signal / noise ratio	56 dB
Sensor gain	86 $mV/decade$
Smallest detectable irradiance	$< 10^{-3}\, W/m^2$
Pixel clock	$> 4\, MHz$
Frame rate	$> 150/s$

V. Summary

In this paper a random addressable imager has been described. The output characteristic shows a logarithmic response for seven decades of light intensity. The combination of high pixel bandwidth and row readout preselection enables realization of fast low power imaging devices in standard CMOS technology that exhibit high speed even at low irradiance.

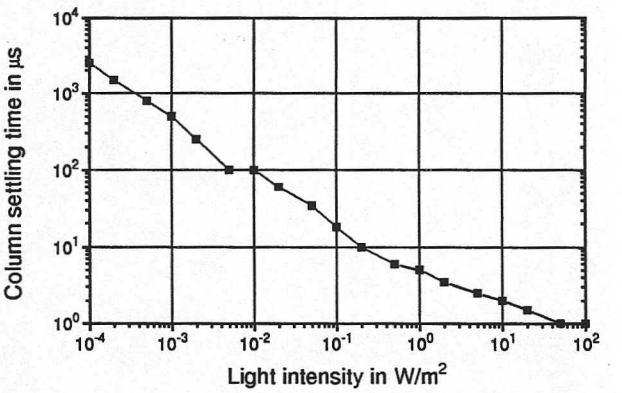

Fig. 6. Settling time after column address change without preselection operation

FPN corrected, aperture correction

Fig. 7. Portraits of four of the authors

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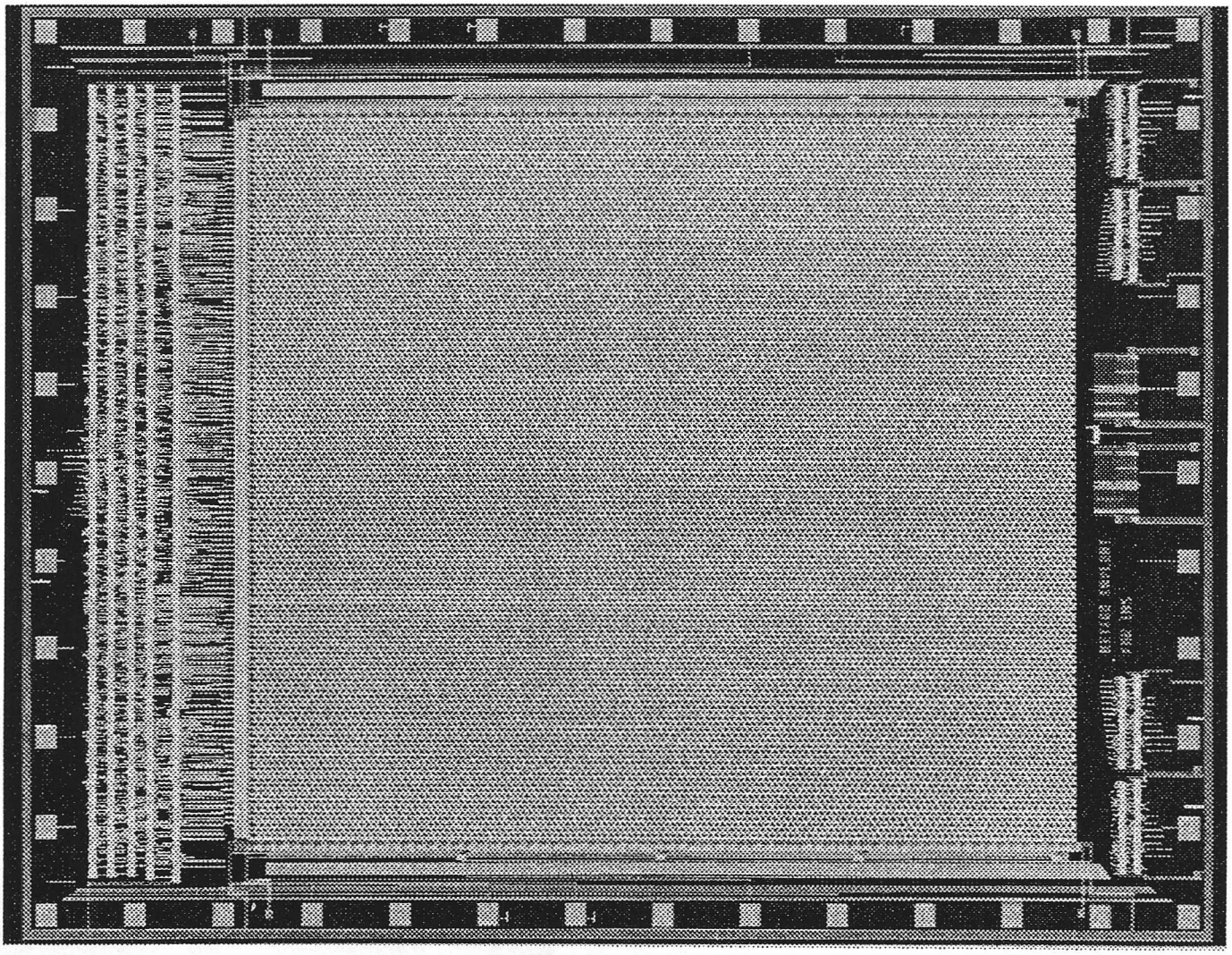

Fig. 8. Chip photomicrograph

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