A 1/4 Inch 330k Square Pixel Progressive Scan CMOS Active Pixel Image Sensor

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ABSTRACT

This paper introduces the first consumer-use 1/4 inch 640(H)x480(V) pixel Active Pixel Sensor with 5.6x5.6 um^2 pixel size. The imager operates with a 5.0 V single power supply and the power dissipation is less than 30 mW. The sensor has been fabricated with 0.6 um, double poly-silicon, triple metal CMOS process technology.

INTRODUCTION

The CMOS active pixel sensors(APS) have attracted special attention in the recent year because of monolithic integration of controlling, driving and signal processing circuitry within a single sensor chip. Several reports on APS have been presented to date[1,2,3,4,5]. However, a large pixel area is required for implementing row select, charge reset and amplification elements in a pixel. The pixel size is limited by the size of these elements. A further pixel size shrinkage is necessary, especially for applications like consumer-use digital still photography.

In this paper, we have studied several different pixels circuits to achieve a smaller pixel size. Similar work aiming to reduce the cell size was reported for the television system, however, the device operated only in the interlace scan mode.

This paper introduces the first consumer-use 1/4 inch 640(H)x480(V) pixel Active Pixel Sensor with 5.6x5.6 um^2 pixel size. The imager operates with a 5.0 V single power supply and the power dissipation is less than 30 mW. The sensor has been fabricated with 0.6 um, double poly-silicon, triple metal CMOS process technology.

DESIGN CONSIDERATION

Three different types of cell structure have been studied in this work.. Figure 1 shows a comparison of the cell structures. The cell structure of transistor address type has three transistors. A transistor (SL) is used for activating the source follower and address the selected line. Next, the cell structure of capacitor address type has two transistors and one capacitor. In this structure, the select transistor is omitted. Last, the cell structure of one transistor, capacitor address type has one transistor and one capacitor. The reset transistor is omitted.

The minimum cell layouts for each type of cell circuit are also shown in Figure 1. The gate, source, drain, photo-diode and separation region are expressed as a square block units. The hatched area represents the gate electrode and the plain area represents LOCOS region. The symbol "PD" shows photodiode. The width of each block represents the minimum lithographic pattern. Each block is piled up and the active regions are formed along a straight line as shown in Figure 1. We have found that these simple

layouts realize the minimum cell size. The cell size for the transistor address cell, capacitor address cell and one transistor 1 capacitor cell are $16F^2$, $14F^2$ and $14F^2$, respectively. F is the minimum length of the design rule.

The minimum size layouts shown in Figure 1 stretch vertically. Therefore, the horizontal image resolution is much higher than the vertical one. These layout are not suitable for square pixel, which is required for multimedia application. We propose a new zigzag layout. An example of a zigzag layout is shown in Figure 2. The layout uses the same pixel structure shown in Figure 1. The even columns and the odd columns are shifted by half a pitch, alternately, in the vertical direction. A photodiode is arranged in every square unit block using this zigzag layout. The broken line in Figure 2 shows two neighboring unit pixels.

Figure 3 shows the block diagram of the chip. The vertical register sequentially selects a single row line for signal read-out processing. The signal charge generated at the photo-diodes is buffered in the primary source follower amplifier in each cell. The source follower load transistor for each column line is located in the upper side of the cell array. The output signal from the pixel circuit is buffered and linked to 1H-memory via sampling enable switch. The signal sampled in the bottom memory are sequentially read to the output amplifier by the horizontal register, located at the bottom part.

FABRICATION

A transistor address cell is adopted for the sensor. The sensor was fabricated with 0.6 um, double poly-silicon, triple metal CMOS process technology. The color filter array and micro lens have been formed on the sensor. Figure 4 shows the reproduced image of a resolution chart. A micrograph of the chip is shown in Figure 5. The sensor characteristics are summarized in Table 1.

CONCLUSION

A 1/4 inch 640*480(V) pixel Active Pixel Image Sensor with 5.6×5.6 μm has been newly realized. This sensor operates with a 3.3V single power supply and the power dissipation is less than 30 mW.

The saturation level is 700mV and the fixed pattern noise at 60C is $10mV_{p\text{-}p}$.

REFERENCES

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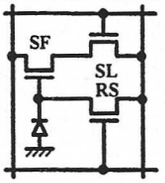
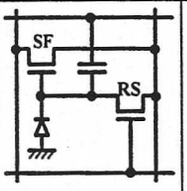
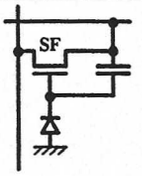
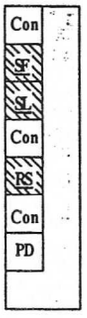
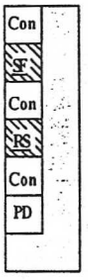
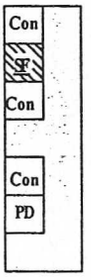
Cell Types	Transitor Address Type	Capacitor Address Type	1Tr・1Cap Type
Transitors/cell	3	2	1
Capacitors/cell	0	1	1
Contacts/cell	3	3	3
Circuits			
Mimimum Layout			
Minimum Cell Size	$16F^2$	$14F^2$	$14F^2$

Figure 1:APS Cell layout for minimum size layout.

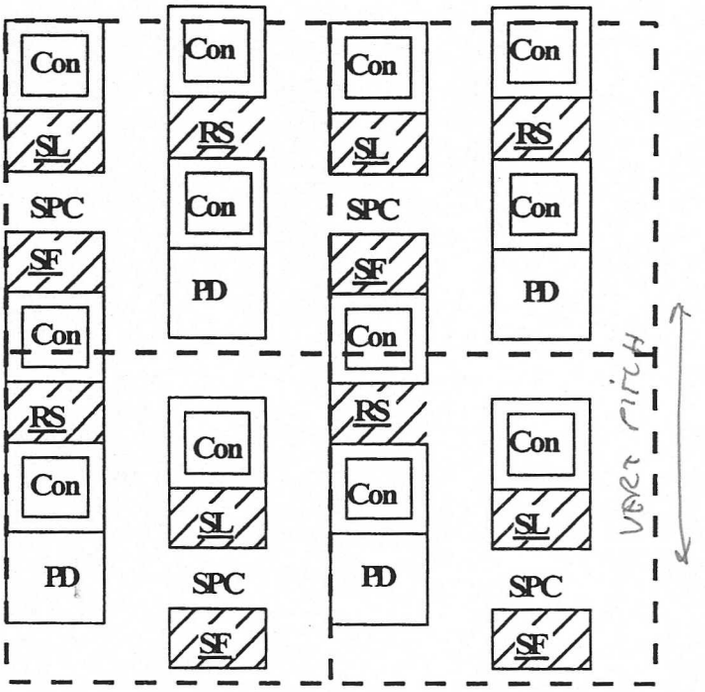


Figure 2:Schematic layout of the zigzag cell.

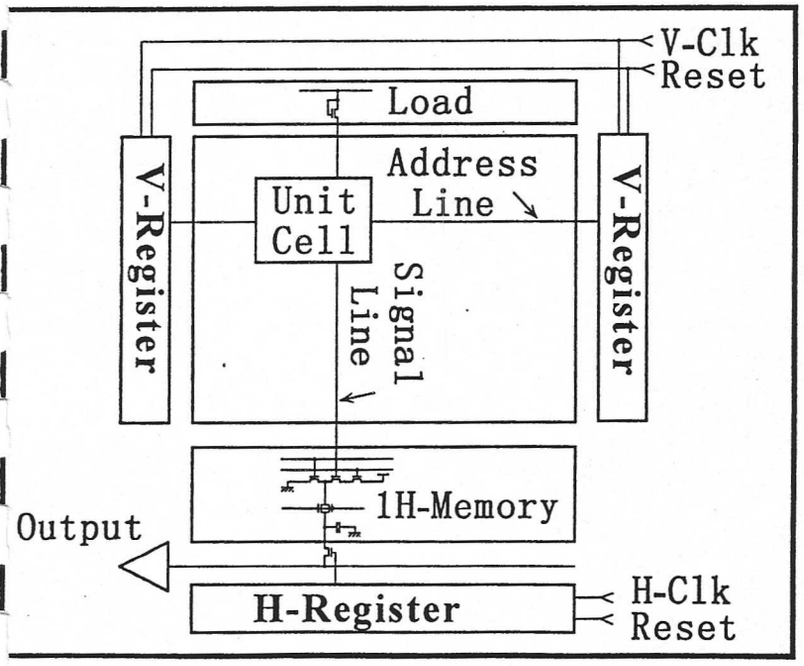


Figure 3:Block diagram of the sensor chip.

Optical Format	1/4 inch
Effective Pixels	640(H)×480(V)
Pixel size	5.6×5.6 μ m²
Photodiode area	1.7×3.1 μ m²
Aspect Ratio	4(H)×3(V)
Image area	3.52×2.64 mm²
Die size	6.4×5.4 mm²
Process	CMOS Technology
Design Rules	0.6 μ m
Saturation Level	700 mV
FPN	1.0mV p-p (at 50 ℃)
Frame Rate	30 Hz
Power Supply	5.0 V
Power dissipation	30 mW

Table 1: Summary of Characteristics

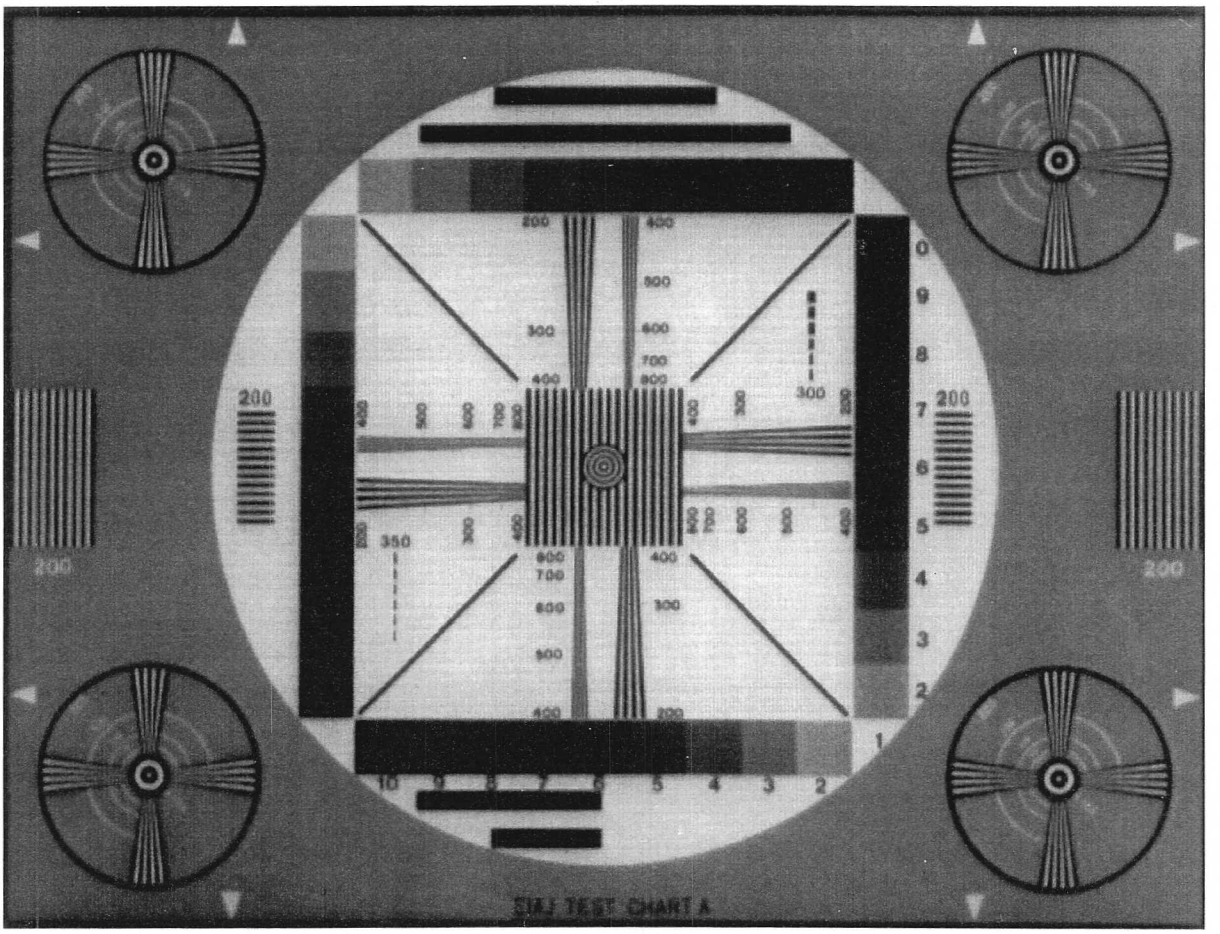


Figure 4: Reproduced image.

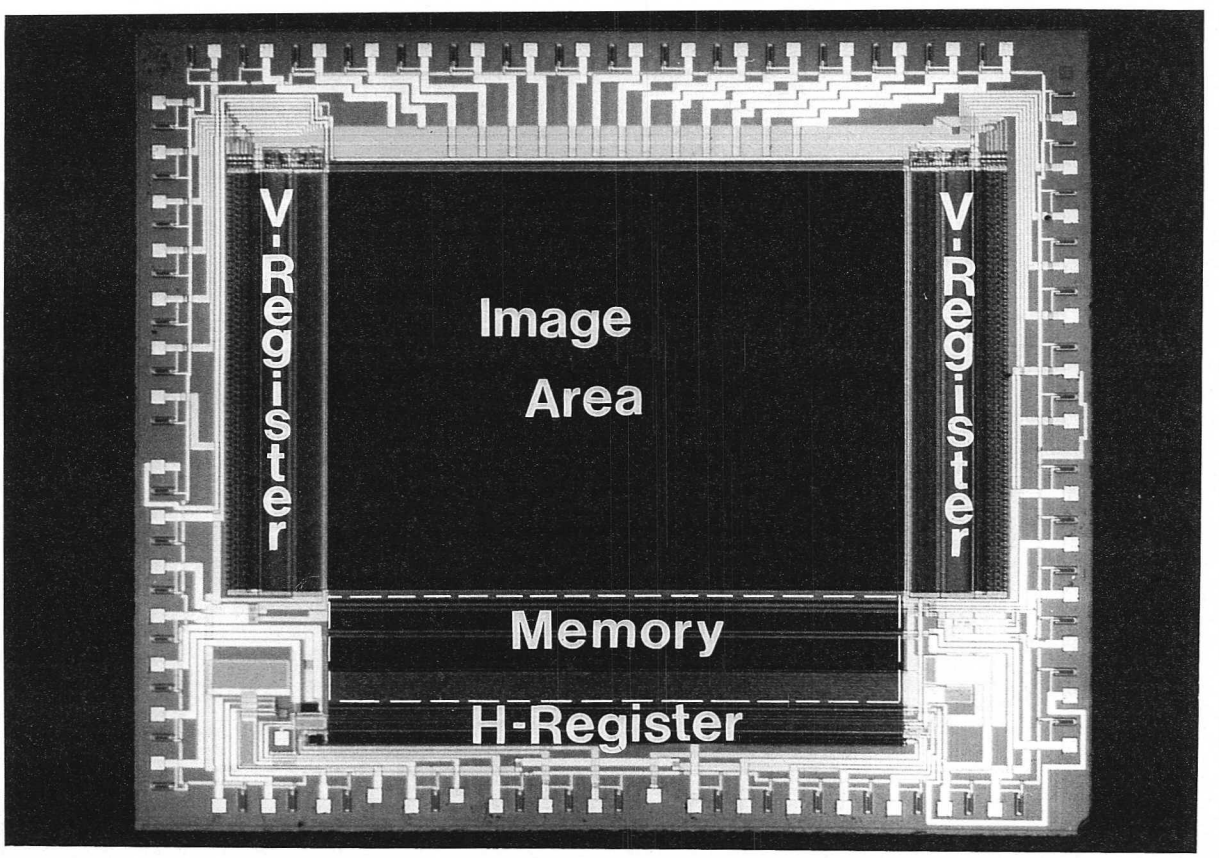


Figure 5: Micro Photograph of the APS chip.