Low Noise and High Speed Charge Detection in High Resolution CCD Image Sensors.

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Abstract:
This article analyses problems associated with low noise and high speed charge detection encountered in high resolution image sensors. It is shown that the conventional Floating Diffusion (FD) charge detection concept is inferior to the previously studied Floating Gate (FG) approach. A new output charge detection well reset technique and an improved biasing method allowed to design the FG charge detection amplifier with a conversion gain comparable to FD structures but with a better noise performance at the data rates up to 40MHz.

The theoretical analysis of the FG concept is confirmed on a 1000 x 1000 Frame Transfer image sensor. The new sensor does not need the conventional CDS circuit for the signal processing, since the FG detection node is sensing charge nondestructively without generating kTC noise. The described progress in the FG charge detection sensing thus opens up a possibility for designing of distributed FG Amplifiers that can theoretically reach the ultimate low noise performance.

Introduction:
The Floating Diffusion structure (FD), introduced into the CCD technology at its early development stages, has been highly developed and is the most widely used device for charge detection in CCD image sensors. However, it seems that further improvements are slow and that many researchers are turning to other structures attempting to outperform the traditional FD charge detection amplifiers (2,3).

The main problem with the FD is that charge is sensed destructively. The FD is typically an N+ node which is reset to a reference voltage. This results in "kTC" reset noise (4). The reset noise can be "eliminated" or minimized by a signal processing technique known as Correlated Double Sampling (CDS) (5). However, this technique requires additional circuitry which is frequently added off-chip, and which requires a wider bandwidth that ultimately leads to a higher noise floor. Of course, kTC noise can not be completely removed and a residual component of it is added to the sensor noise floor together with other contributions such as the reset transistor partition noise (6). The problem of the large noise floor is more pronounced in high resolution image sensors that have to operate at high frequencies to process signals form more pixels in the same scanning time.

The purpose of this article is to investigate the formerly developed but not frequently utilized Floating Gate (FG) charge detection structure and show that it can outperform the FD structure in a typical high resolution image sensor. It will also be shown that the CDS signal processing method, while reducing kTC noise, increases noise generated in the first buffer amplifier stage and thus should not be used if the lowest charge detection noise floor is desired. Finally it will be suggested that the best charge detection performance can be achieved with the Distributed Floating Gate Amplifiers (DFGA) investigated many years ago (7).

Floating Diffusion and Floating Gate Cross Sections:
For an easy comparison the cross sections of the FD and the new FG structures, with an accompanied potential profiles, and as implemented in the Virtual Phase (VP) technology, are shown in Fig. 1. The VP FD structure is standard, formed by an N+ diffusion surrounded by a poly gate which is connected to it (8).

The VP FG structure is new and shows two new elements. The first is the resistive reset gate. It is formed by a typical VP P+ gate to which a metal contact has been added in the middle of the CCD channel. When a positive biasing pulse is applied to it a hole current flows through the gate to the P+ channel stops located in front and behind the plane of drawing. Since the gate has a relatively high resistivity and is usually only one in the entire image sensor array, the added power dissipation is negligible. An advantage here is that the reset gate is selfaligned to the FG which minimizes overlap capacitances present in the multiphase technologies. This feature also reduces the feedthrough. The second important element in the new FG structure is the biasing element. It is essential for a high quality image formation to establish a stable DC level on the floating gate and maintain it throughout the readout time. This can be accomplished by several ways: A direct approach is to connect an MOS reset transistor to the gate and pulse it at suitable intervals such as during the horizontal blanking. However, the MOS transistor is large and would add an unacceptable parasitic capacitance to the node thus lowering the FG conversion gain below that of a typical FD. For this reason a new approach selected here was to use a diode. The diode can be designed very small and

since the voltage swing from the signal charge under the FG is always negative the polarity can be chosen such that the diode is always reverse biased when charge is sensed. The diode can be reset to any desirable level by a positive pulse applied during a suitable time interval.

FG noise analysis:

It can be shown that noise contributed by the biasing diode is negligible since the diode reverse leakage current is very small. The only significant noise source in the FG amplifier is thus noise generated in the buffer MOS FET transistor. It has usually two main components: Johnson noise and 1/f noise. 1/f noise can be particularly troublesome in the video systems, since it is highly visible on the TV screen. The common practice to avoid this problem is to use an AC coupling somewhere in the video chain and a DC restoration at every horizontal TV line.

In this work the line clamping approach is modified and the DC level is restored at every pixel in correlation with the clocking similarly as in the CDS approach. The Correlated Pixel Clamp (CPC) signal processing method, however, may increase noise if the circuit is not optimized. To understand this point more clearly a simple circuit model shown in Fig. 2 is considered. The resistor R could also be connected in series with the switch to keep it out of the signal path. Moreover the capacitor value can be selected large and the resistor value small such that noise from the resistor is negligible relative to $v_n(t)$. Using the circuit equivalent configuration, also shown in Fig.2, it is possible to write equations for the voltages $v_s(t)$ and $v_c(t)$. From these expressions it is then possible, after some algebraic manipulations, to write perhaps an intuitively obvious formula for the noise variance of the sampled and held output signal:

$$< v_h^{\,2} >= S_0 \cdot \pi \cdot (\omega_b + \omega_f). \qquad (1)$$

Here S_O represents the input white noise power spectral density, $\omega_f = (R \cdot C)^{-1}$, and ω_b is the base-band angular frequency of a filter which is inserted just prior to the sampling and holding circuits. Equation (1) is very useful in understanding the difference between the CDS and the CPC noise performances. In the CDS signal processing method it is necessary to have both ω_b and ω_f equal and wide open in order to properly remove kTC noise. Thus the CDS, while minimizing kTC noise, is more than doubling Johnson noise of the buffer MOS FET transistor. The base-band filter bandwidth for an efficient CDS performance needs to be considerably wider than it would be to pass only the signal alone. In many systems it is common to find that at least $\omega_{b(CDS)} = (3/2) \cdot \omega_{b(CPC)}$. In the CPC signal processing method, on the other hand, ω_b needs to satisfy only the minimum bandwidth requirement and ω_f needs to be as low as possible not to significantly contribute to the noise floor, but wide enough to efficiently minimize 1/f noise.

From the above, somewhat abbreviated analysis, considering the best case of an ideal CDS with a complete kTC noise removal and no partition noise, it can be concluded that the CPC will theoretically outperform the CDS by a factor of:

$$F_n = \sqrt{\frac{< v_h^{\,2} >_{CPC}}{< v_h^{\,2} >_{CDS}}} = \sqrt{3}/3. \qquad (2)$$

In practice, however, this factor is usually far less than 0.577, since in high resolution image sensors, which have to operate at high clocking frequencies, the CDS noise reduction capability is further impaired by the necessity to open up ω_b beyond the factor of 3/2 to compensate for the time intervals consumed by the CCD clocking transitions.

Implementation of the FG amplifier in a high resolution image sensor:

The layout of the high resolution image sensor selected as a test vehicle for the FG concept is shown in Fig. 3. It is a conventional Frame Transfer (FT) device with 1000 active lines and 1000 active pixels in each line. The pixel size in the image sensing area is 8.0 microns in both horizontal and vertical directions. Several improvements and new features can be noted in this design. The first improvement is the introduction of the image area vertical bussing lines. These are aluminum and are connecting either the poly gates or the antiblooming devices alternately to the top cross busses. This improvement allows the sensor vertical transfer rate to be as high as 10 MHz.

The second new feature is the lateral overflow antiblooming device. It is formed by a small circular poly ring with an N+ drain in the center which replaces every other channel stop. To form the antiblooming barrier a suitable boron implant is placed under the poly as indicated in the insert in Fig. 3. The blooming barrier allows the gate to be directly connected to the N+ drain by the same metal line without charge injection form the drain back to the CCD channel. A suitable bias applied to this antiblooming device controls the charge overflow level and it can also be used to clear charge from the pixels completely if the bias is pulsed high enough.

The third new feature introduced in this sensor is the layout of the serial registers and the accompanied vertical transfer gates. The details of the layout are given in the second insert also shown in Fig. 3. Two registers, each with two phases, were used and are

connected as indicated in the drawing. When charge is transferred from the memory, even column charge ends up in the lower register while the odd column charge remains in the upper register. The registers are then clocked with a complementary clocking pulses with the 50% duty cycle. This arrangement allows to transport charge with only 20MHz clocking frequency, but with the data rate of 40 MHz. A clearing drain was also incorporated into the design, below the serial registers, to facilitate the fast charge clearing from the memory.

The fourth new feature is, of course, the FG amplifier itself. The nondestructive charge detection mechanism was helpful here in selecting the amplifier topology. By operating the reset gates with complementary pulses and again with the 50% duty cycle it was possible to use only a single floating gate for detection of charge in both registers. The key advantage of this approach is that charge from either register is detected on the same gate and buffered by the same transistor. This eliminates problems with channel matching. Since no CDS is required for processing of output signal from this sensor, the necessary bandwidth is achieved by a simple dual stage source follower common to most of the state-of-the-art CCD image sensors.

Discussion of the test results:

The fabricated image sensor was evaluated for all typical CCD parameters and the test results are summarized in Table 1. There were no unusual problems with the operation of the Floating Gate Amplifier other than that it was necessary to make sure that the diode biasing node is shielded from impinging light.

During the evaluation the detail attention was paid to the output signal waveform and noise. The output signal from the CCD was measured directly after a unity gain buffer stage and showed an exceptionally small feedthrough due to the exact cancellation of the out-of-phase clocked reset pulses.

The most important amplifier parameter is the noise floor. This was measured using the Tektronix spectrum analyzer and the noise equivalent electron value was extracted by integrating the spectrum. The result is given in the Table 1 together with the sensor conversion factor. The obtained noise floor of $N_{ee} = 42e$, is a relatively large number traced back to a large parasitic capacitance of the biasing diode. This problem has been corrected in the subsequent sensor fabrication cycles and the new result is also shown in Table 1.

Future development:

The nondestructive charge detection sensing allows to consider the design of distributed amplifiers(7). An example of a block diagram of such a Distributed Floating Gate Amplifier design that can be easily implemented in the VP technology is shown in Fig.4. In this example only four stages are shown, but it is clear that this concept can be extended to as many stages as necessary.

The distributed amplification in CCD devices has many advantages: The first one is the increase of the signal to noise ratio. As can be seen in the diagram in Fig.4 the charge signal which arrives at the common detection node at the end of each channel sums coherently, while the contributions from Johnson noise generated in MOS FET transistors sum randomly. This improves the S/N ratio by a factor of $\sqrt{N}$, where N represents the number of stages. Of course it is necessary that noise associated with the charge input into each channel is smaller than Johnson noise from the FG amplifiers. This is no problem, since the size of the channel registers can be increased as needed to satisfy this condition. The second advantage of the DFGA is the speed. The amplification is accomplished synchronously with the clocking. The third advantage is the large off-chip driving capability and a large gain. Since charge has been amplified, and many channels summed together at the output, only a single large transistor stage is needed to drive the off-chip circuitry.

In conclusion, it is clear that the DFGA is the amplifier of choice for the future high performance CCD image sensors.

Conclusions:

In the above described analysis it has been shown that in order to achieve the lowest charge detection noise floor, the CDS signal processing method should be replaced by the CPC signal processing which can be used with FG amplifiers. The CDS signal processing while minimizing kTC noise more than doubles Johnson noise generated in the buffer MOS FET transistor. The FG concept has been verified on a high resolution high performance FT image sensor. Several new features of the sensor have also been presented and described in detail. Finally, a conclusion has been reached that the ideal charge detection amplifier for the future high resolution and high performance CCD image sensors, that have to operate at high clocking speeds, is the DFGA.

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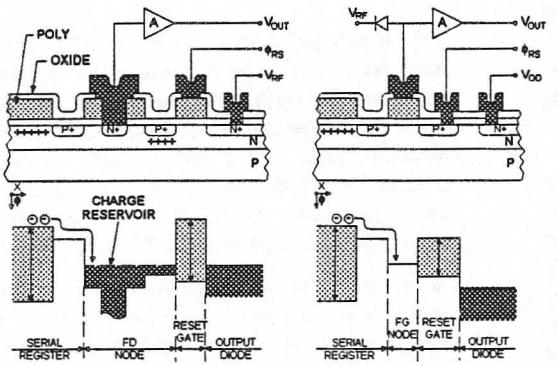

Fig. 1. Device cross section with potential profiles for a standard VP Floating Diffusion and the new Floating Gate charge detection nodes.

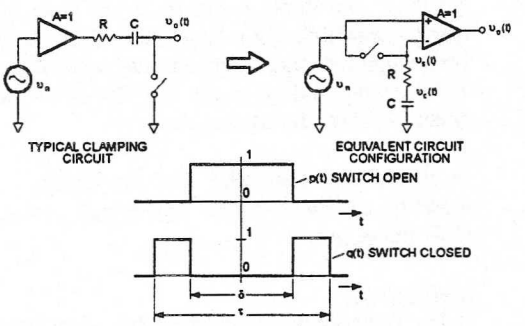

Fig. 2. The typical Correlated Pixel Clamping circuit and its equivalent configuration used for the noise calculations with the corresponding timing diagram.

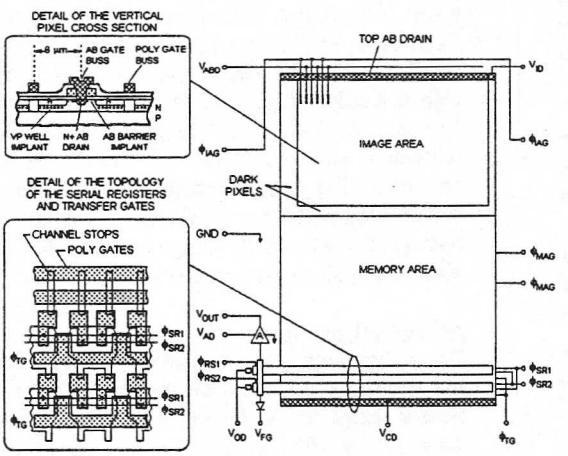

Fig. 3. The basic topology of the FG test image sensor showing detail cross section of the antiblooming device and the details of the serial register layout.

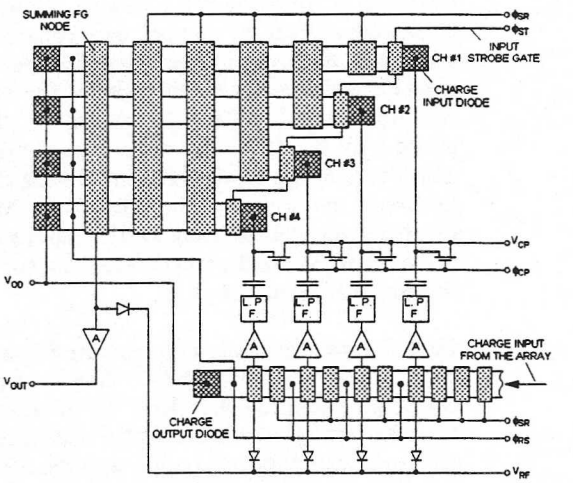

Fig. 4. Proposed circuit diagram for the Distributed Floating Gate Amplifier.

Table 1. TC281 Image Sensor Specifications and Test Results.

Parameters	Values	Parameters	Values
Chip Size [mm]	9.0 x 15.8	Conv. Gain [uV/e]	4.1(8.2)
Total Pixel Num.	1036 x 1010	Well Capacity [ke]	24.0
Active Pixels	1000 x 1000	Dark Current [pA]	70
Pixel Size [um]	8.0 x 8.0	Noise Floor [e]	42(21)
Vertical Cl. Rate	5(10) MHz	Dyn. Range [dB]	54(60)
Horiz. Cl. Rate	20.0 MHz	Sensitivity [mV/L]	120(240)
Saturation Output	100(200) mV	Antiblooming	2000 x
			(second run values)

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10 V clocks