A High Performance 5V-Only 1/5-Inch 220k-Pixel CCD Image Sensor

Takashi Watanabe, Eiji Koyama, Kengo Yamamoto, Eiichi Akaike,
Satoru Takano, Tuguhisa Inoue, Koji Okada, Takayuki Kawasaki,
Hiroshi Urabe, Hiroshi Adachi, Junichi Nakai, Kiyotoshi Misawa

Logic IC Engineering Center, Tenri IC Development Group, Sharp Corporation

ABSTRACT

We developed a high performance 5V-only 1/5-inch 220k-pixel IT-CCD image sensor by incorporating high efficiency charge pump circuits, pulse mixing circuits, level shift circuits and driver circuits. This device reduces power consumption, number of parts and volume of camera systems drastically, and has such applications to small and mobile video communication tools.

1. Introduction

Recent interline transfer (IT) CCD area image sensors have attained very high sensitivity and low noise in small pixel size about 5μm square by adopting such technologies as buried photodiode, microlens, and high gain charge detect amplifiers[1]. Those devices, however, usually need many driving voltages from high to negative value to attain high sensitivity and sufficient dynamic range. CMOS image sensors are one possibility to achieve low voltage and low power consumption [2], but the S/N of those devices is obviously behind the CCD.

To combine low power consumption with high performance, we developed a 5V-only IT-CCD image sensor by incorporating high efficiency charge pump circuits, pulse mixing circuits, level shift circuits and driver circuits. The details of those circuits and the technology to combine them with CCD imaging part will be further discussed in this presentation.

2. Technology of 5V-only power supply

Fig.1 shows the block diagram of a 5V-only CCD imager. The device is formed from two parts; sensing part and driving part. The driving part consists of charge pump, pulse mixing, level shifiting and driver circuits, which are driven by 0-5V external pulses and 5V DC supplies. The sensing part is a 1/5-inch 220k-pixel IT-CCD.

(A) Charge pump circuits

Fig.2 shows Dickson voltage multiplier[3]. As maximum generated voltage is restricted by pulse hight and body effect of MOS FET[4], we employed punch-through type MOS FET which is shown in Fig.3.

Power efficiency η of the circuit is descrived as;

$$\eta = I_o \cdot V_o(I_o) / (I_o \cdot V_o(0) + \Sigma_i (C_{Gi} \cdot V_{\phi i}^2 \cdot f)) \quad (1)$$

where I_o is output current, $V_o(I_o)$ and $V_o(0)$ are output voltage at I_o and $I_o=0$ respectively, C_{Gi} is gate capacitance of MOS FET, $V_{\phi i}$ is clock pulse hight, f is clock frequency, and i indicates each stage. The first and the second terms of the denominator of eqation (1) show DC and AC input power respectively. The DC power efficiency depends on the voltage drop from $V_o(0)$ to $V_o(I_o)$. This drop is caused from two factors as is shown in Fig.4. Namely, one is that the electron charge packet ΔQ which is swept out from source per one clock cycle lowers drain potential by $\Delta V_1 = \Delta Q/(C_o+C_G)$, where C_o is coupling capacitance in Fig.2 and C_G is gate capacitance of MOSFET. The other is that the electron flow ($-I_D$) from source to drain requires the potential difference ΔV_2 between source and the channel under the gate. ΔV_2 can be calculated from MOS FET characteristics, effective time of current flow and the charge of ΔQ. ΔV_1 and ΔV_2 are reduced by increseing C_o and W/L of MOS FET, respectively. To minimize $\Delta V_1 + \Delta V_2$ in restricted chip area, we optized C_o and W/L. Fig.5 shows the relation between $\Delta V_1 + \Delta V_2$ and I_o in two cases on the same chip area. We obtained total power efficiency as η=52% at I_o=200μA, hence power loss in the circuits 3mW which is trivial in a camera system.

In Fig.2, pumping clocks ϕ_1 and ϕ_2 are common to horizontal CCD clock and reset clock to avoid those clocks interfere with CCD imaging part.

(B) Pulse mix and level shift circuits

Fig.6(a) shows a new pulse mixing circuit which uses CMOS FETs. This circuit generates three level pulse from two level input pulses and can shift the high level from 5V to VH (>5V) and low level from 0V to -VL (<0V). The timing diagram is also shown in Fig.6(b).

3. Combine with high performance CCD

(A) Pixel structure

Fig.7 shows a cross sectional view of the IT-CCD imaging pixel. The photo diode (PD) and the vertical CCD (VCCD) are formed in shallow flat P-well(PW1) [5]. Another Pwell (PW2) and P^+ layer are formed at bottom of the VCCD and at surface of the PD, respectively. A doping profile of the PD is optimized by using high energy ion implantation. As a result, the signal charge in the PD is read out to the VCCD completely or it is swept out to the substrate completely at the shuttering, under the condition of driving voltage which is generated by charge pump circuits in each case. A doping profile of the VCCD is also optimized to maintain sufficient handling signal charge and to reduce dark current when the VCCD is driven at 5Vpp pulse. Two layers of metal optically shield the VCCD to reduce the smear signal and the resin microlens covers each PD to rise the sensitivity.

(B) Well structure

The pulse mixing circuit employs CMOS FETs, therefore it needs P-well and N-well whose electric potential must be independent from that of N-substrates. As the potential of the N-substrate changes strongly at shuttering mode, we introduce a P^+ layer at the bottom of the P-well by high enery ion implantation, and the N-well is formed at upper layer of the P-well. We obseved no detrimental phenomena such as latch-up.

(C) Reset auto biasing circuits

The use of the charge pump circuit for a reset drain enables self biasing of a reset clock pulse. Fig.8 shows the reset auto biasing circuits. The channel structure of the final stage MOS FET in the charge pump circuit is the same as that of the reset gate, and the source of the MOS FET which act as the output of the pump is connected to the reset drain. Therefore, the voltage of reset drain is just the same as the channel conducting potential of the final MOS FET when external clock ϕ_R is high. This means that the channel potential of the reset gate is just conducting condition for the reset drain voltage when external clock ϕ_R is high.

4. Characteristics

The main characteristics of a 5V-only 1/5-inch 220k-pixel IT-CCD image sensor are summerized in Table 1. Sufficient value for a video camera use are obtained, even though 5V single voltage supply and small optical area. The power consumption of this device is about 1/3 of that of conventional CCDs, and by using this device, camera parts and camera volume are drastically reduced as 62% and 40% of those of conventional CCD cameras, respectively.

5. Conclusions

The incorporation of high efficiency charge pump circuits, pulse mixing circuits, level shift circuits and driver circuits with a 1/5-inch 220k-pixel IT-CCD image sensor yields excellent results for 5V single voltage power supply. This device reduces power consumption, number of parts and volume of camera systems drastically, and widen applications to small and mobile video communication tools.

References

[1] T.Ozumi et al., "A 1/4-type 410-k pixel IT-CCD image sensor", Sharp Technical Journal, vol.60, p.37, Dec. 1994

[2] E.Fossum, "CMOS image sensors: Electron camera on a chip", Int. Electron Device Meet., p.17, 1995

[3] J.Dickson, "On-chip high-voltage generation in MNOS integrated circuit using an improved voltage multiplier technique", IEEE J. Solid-State Circuits, vol.SC-11, p.374, June 1980

[4] J.Witters et al., "Analysis and modeling of on-chip high-voltage generator circuits for use in EEPROM circuits", vol.24, p.1372, Oct. 1989

[5] S.Miyatake et al., "A shallow flat p-well structure for interline trans-fer CCD image sensors", IEEE Trans. Elec.Devices, vol.ED-33, p.458, Apr. 1986

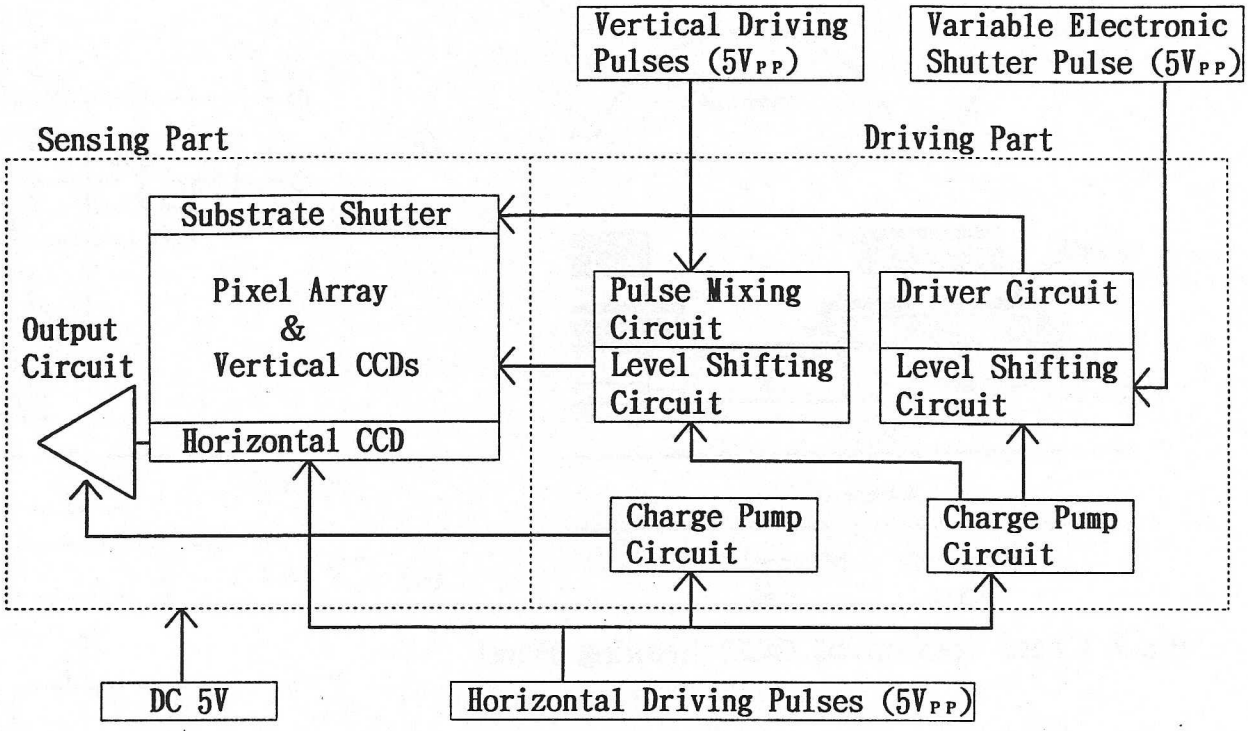

Fig.1 Block Diagram of 5V-only CCD Imager

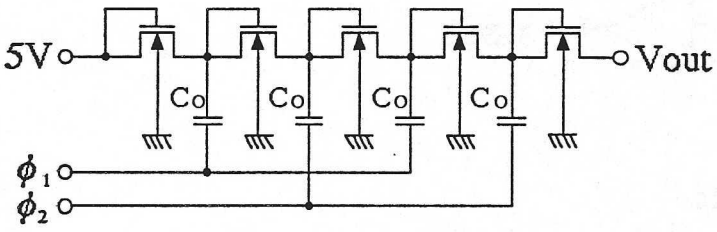

Fig.2 Charge Pump Circuit

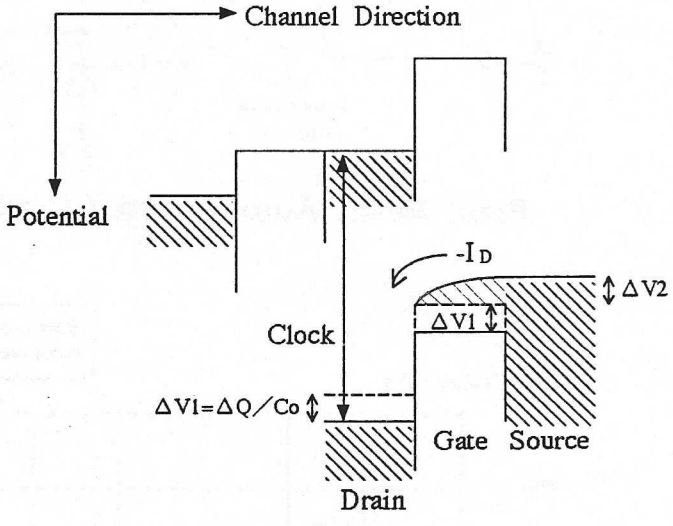

Fig.4 Voltage Drop of Each Stage in Charge Pump

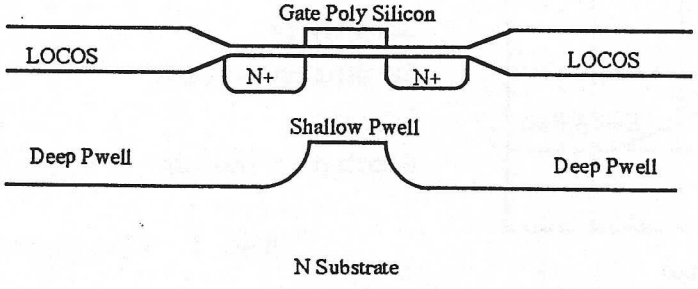

Fig.3 Structure of Punch-through Transistor

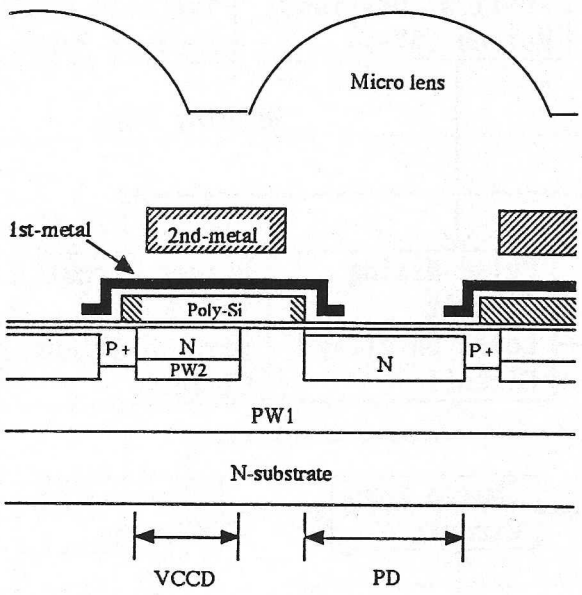

Fig.7 Cross Section of CCD Imaging Pixel

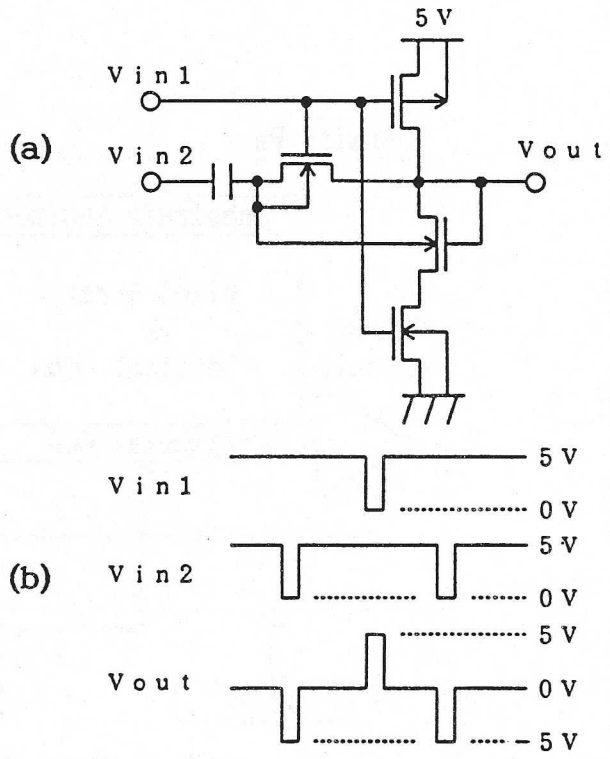

Fig.6 Pulse Mixing Circuit
(a)Diagram, (b)Timing

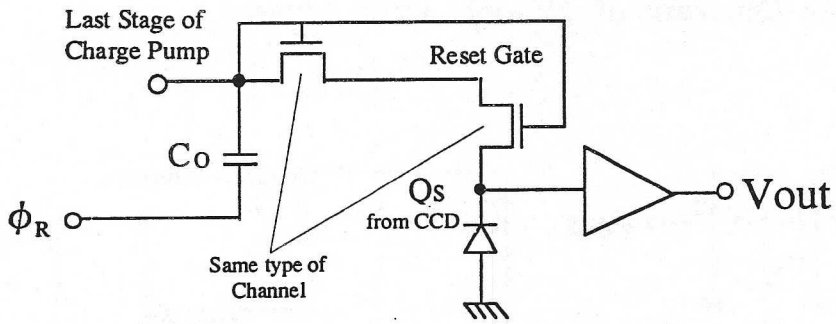

Fig.8 Reset Auto-biasing Circuit

20μV/e⁻
200μV noise

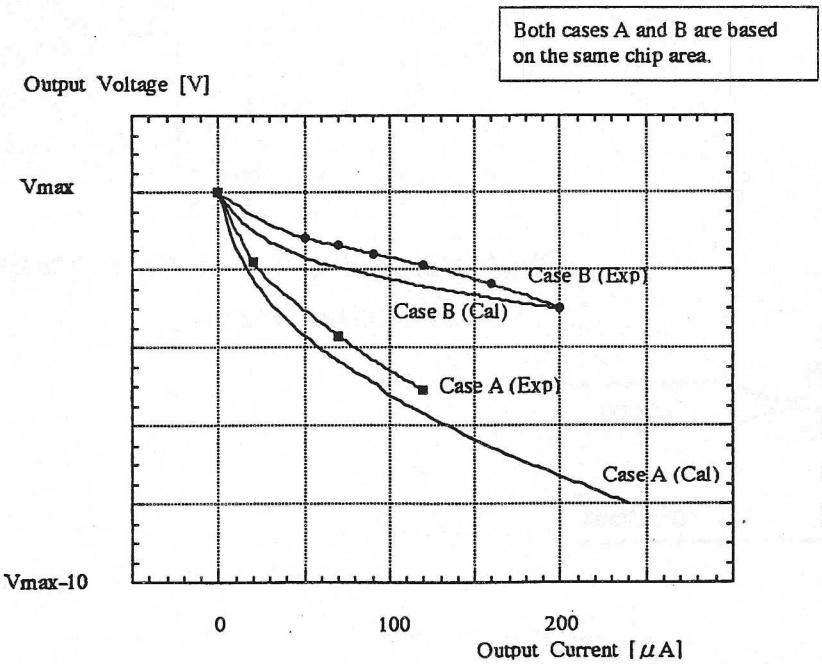

Fig.5 Optimization Effect in Voltage Drop

Power supply	5V only
Optical format	1/5 inch
Effective pixels	362(H)× 582(V)
Total pixels	384(H)× 582(V)
Pixel size	8.2(H)μm × 3.8(V)μm
Sensitivity	50 mV/ℓx
Saturation voltage	600 mV
Smear	-86 dB
Electronic shutter	1/50~ 1/10,000 sec

Table 1 Characteristics