Random noise and fixed pattern noise in STACK-CCD imager

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1.Abstract

The random noise which occurs at a signal charge storage diode has been reduced from 42 electrons rms to 18 electrons rms. The new type cell structure is features with the signal voltage feedback gate(FBG). The FBG is inserted between a stroage diode and a CCD register, and it controls the signal read out channel potential. This channel potential control effect results in a reduction of a signal storage diode capacitance. The random noise is in proportion to a storage diode capacitance, and therefore, it has been decreased as much as by a factor of 2. This random noise will be reduced further more as the cell size is scaled down.

The fixed pattern noise(FPN) has been found to be cased by the variation in the bias charge which was induced in each pixel for the image lag reduction. The bias charge variation has been found to originate from the variation in the read-out transistor for the signal charge. A read-out channel potential fixed operation was able to reduce FPN. The FPN was reduced to 30 electrons peak-to-peak, using this operation.

2.Random noise

The disadvantage of the photoconversion layer overlaid CCD image sensor, as compared with the planer type CCD image sensor, is a random noise which occurs at a storage diode when the signal charge is read out, because the image lag is no longer problem 1)2). The photoconversion layer overlaid CCD image sensor has a great advantage of sensitivity for the planer type sensor. Taking this point into consideration, the photoconversion layer overlaid CCD image sensor is the best type, if provided random noise can be reduced.

The cross-sectional view of the conventional and new type image sensor cells are shown in Fig.1. The new type cell structure is features with the feed back gate(FBG), which is inserted between a stroage diode and a vertical CCD (V-CCD). The storage capacitance is consists of the photoconversion layer capacitance and p-n junction capacitance in the substrate. The equivalent circuit and the potential profile of each process are shown in Fig.2. For the conventional cell, the signal charge(Qsig) is stored in the storage capacitance(Ca), and it is read out into the CCD register by applying a positive pulse on a read out transistor gate. On the other hand, for the new type cell, the FBG is inserted between the Ca and the read out transistor as a feed back transistor and the capacitance (Cf). The total capacitance value(Ct) is serise of Cf and Ca, according to an equivalent circuit analysis.

$Ct=(Cf*Ca)/(Cf+m*Ca)$ m:Channel potential modulation coefficient (m=0.8), and the random noise (Nr) is evalated as

$Nr=\{(KTCt)/2\}^{1/2}$ K:Boltzman constant, T:Absolute temperature.

The Qsig is read out into the Cf by applying a negative pulse on the Ca node. The Qsig is stored in the Cf for a while, and the potential transition is conveyed to feedback transistor gate. The channel potential under the feedback transistor gate is changed to prevent the signal charges moving from the Cf to the Ca. This channel potential change is equivalent to the decrease of the Ca. The potential of the Ca node is risen by applying a positive pulse on another Ca node, before the Qsig is read out. The Qsig in the Cf is transfered to CCD

by applying a positive pulse on the read out transistor gate. The very small random noise is added at this time, but it is negligible, considering very small Cf. The random noise is increased by a fctor of 2, because the bias charge is injected into the storage diode to reduce the image lag 1)2).

The random noise VS storage capacitance(Ca) is shown in Fig.3. The Cf is 1 fF. The random noise is reduced to very low level with this feedback gate structure. The random noise for 5 fF storage capacitance without the feedback gate was, 42 electrons rms. On the other hand, the random noise for the cell with the feedback gate, was as small as 18 electrons rms.

3.Fixed pattern noise

Fig.4 shows a cross–sectional view of a STACK CCD sensor pixel. The STACK CCD sensor has a storage diode reset gate(SRG) and a charge injection diode(CID) for low image lag operation.

Fig.5 shows the potential diagram of a pixel for the image lag reduction operation. After the signal charge and bias charge are read out from the SD with the FSG becoming high(b), the charges are transfered(c). Then SRG is turned on, FSG is high, CID is low and the bias charge is injected into SD(d). At the time, the SD potential is equal to CID potential. The charge in the V–CCD is swept out(e) and the excess charge is drained into CID with FSG going high(f). After reading out the excess charge, the bias charge is left in SD. The bias charge is read out with the integrated signal charge at the next field. In this way, the SD potential is reset for every field, and thus the capacitive image lag is completely eliminated.

The simulated relationship between output voltage(Vout) and input voltage(Vin) at the storage diode is shown in Fig.6. Vout becoms smaller than Vin for the bias charge which is below 100mV. This causes the sensitivity reduction. The Vout increases along with the bias charge increases and coincides with Vin. Then the more than 100mV bias charge is dispensable for good linearity. The FPN was found to be cased by this bias charge variation, then it is very important to suppress this variation.

Fig.7 shows the evaluated FPN for some FSG voltages, with 100mV Bias charge. The FPN was 200 electrons for the FSG voltage is over −1V. On the other hand, the FPN was drastically reduced to 30 electrons for the FSG voltage is lower than −1V. This FPN reduction was accomplished by the suppression of the chort channel effect at a channel under the FSG. With this read–out channel potential fixed operation, it has been possible to reduce FPN to the sufficiently low level.

4.conclusion

The random noise at a signal storage diode has been reduced from 42 electrons rms to as small as 18 electrons rms, for 5 fF storage diode capacitance. The fixed pattern noise has been reduced to 30 electrons for 100mV bias charge. Using this new type cell with the feed back gate and the new operation, the random noise and the fixed pattern noise for the photoconversion layer overlaid CCD image sensor has been reduced to a sufficiently low level.

Reference

1)H.Shibata et al."A 2M–pixel vertically integrated HDTV image sensor".ISSCC Dig. tech. papers. TP11, Feb.1992.

2)M.Sasaki et al."A 2/3–inch 400K pixel stiking–free STACK CCD image sensor". ISSCC Dig. tech. papers, TP12.1, Feb.1993.

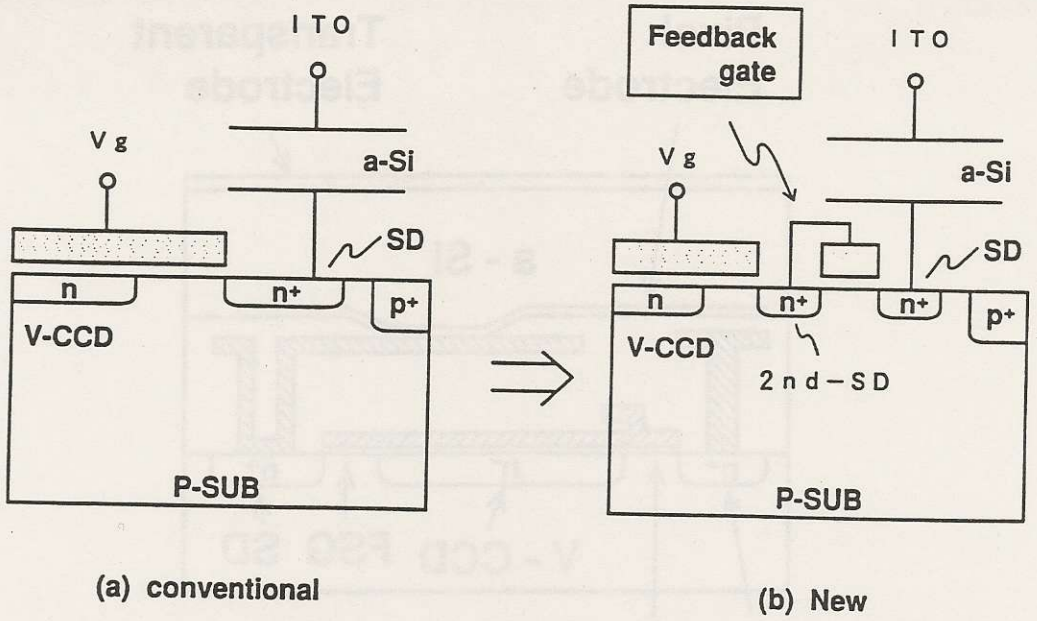


Fig.1 Image sensor cell cross sectinal view

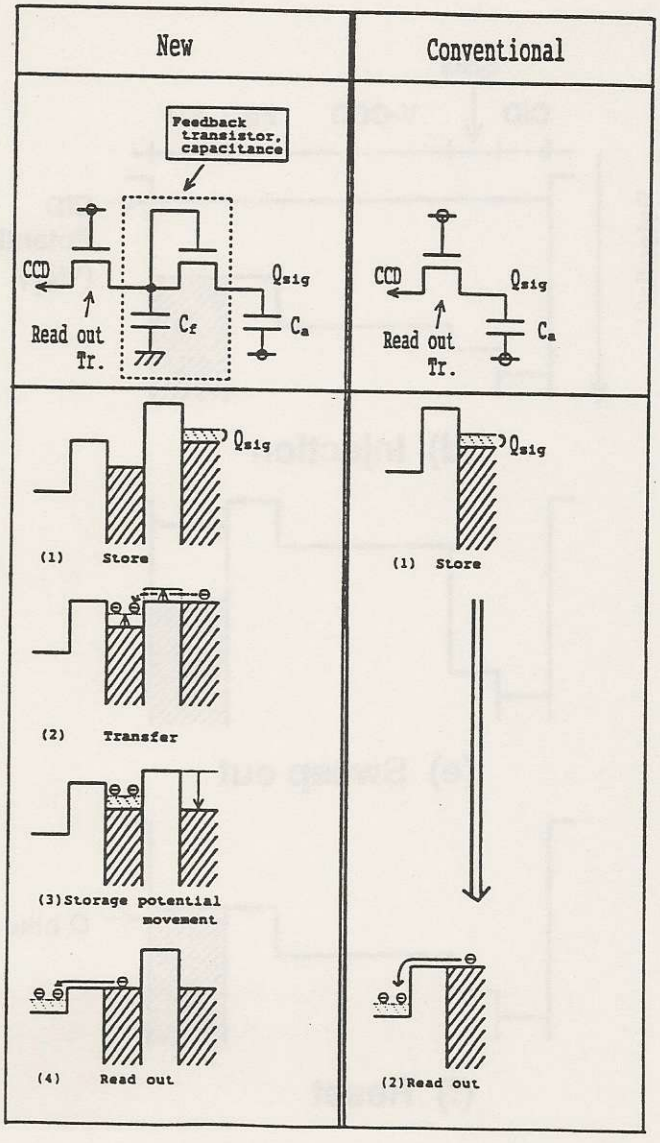


Fig.2 Equivalent circuit

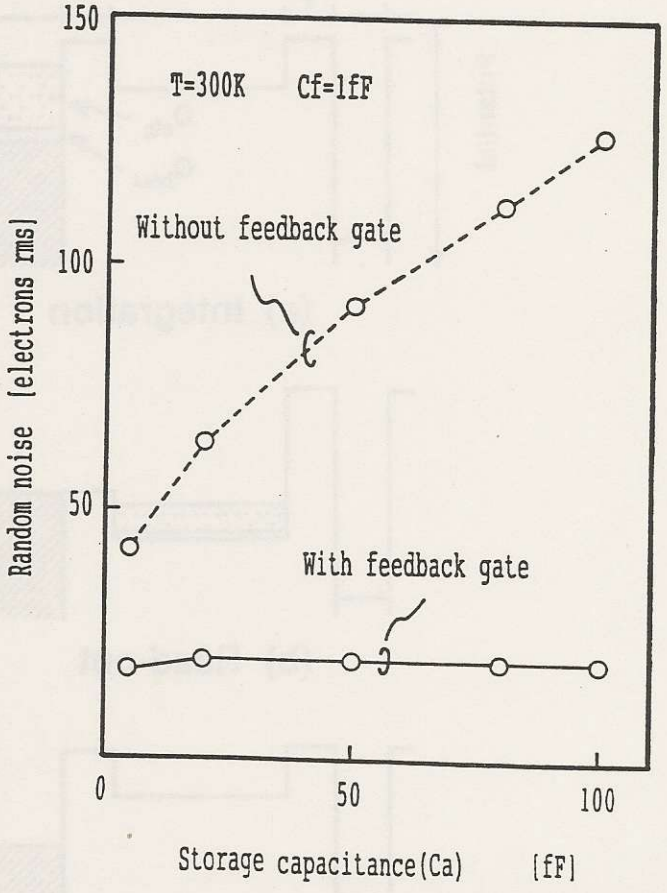


Fig.3 Random noise VS storage diode capacitance

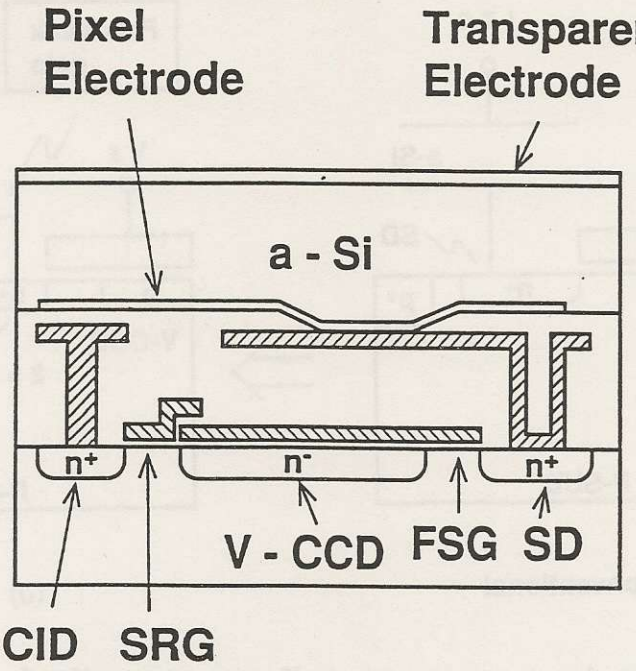
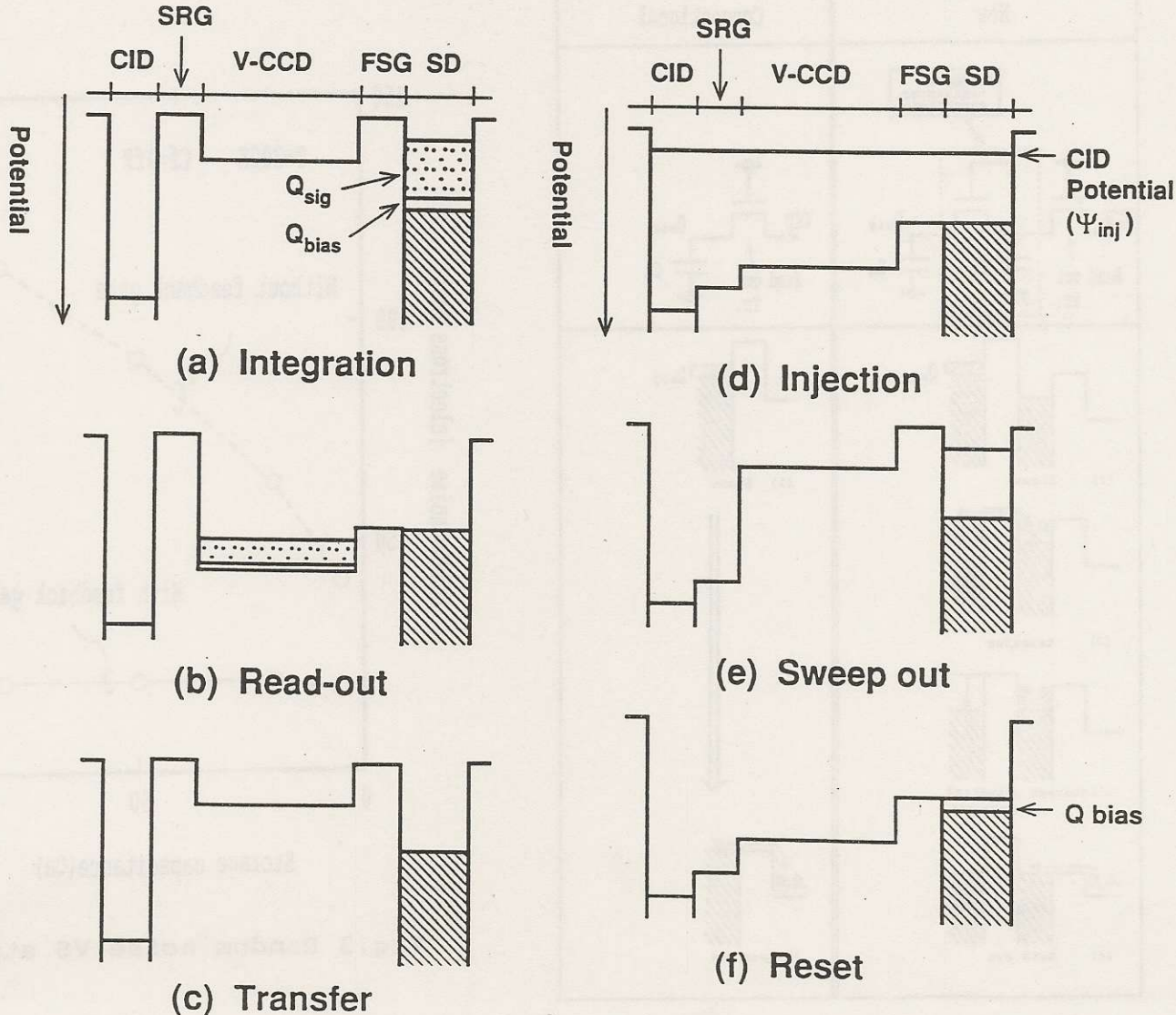


Fig.4 STACK CCD pixel structure



226

Fig.5 Image lag reduction operation

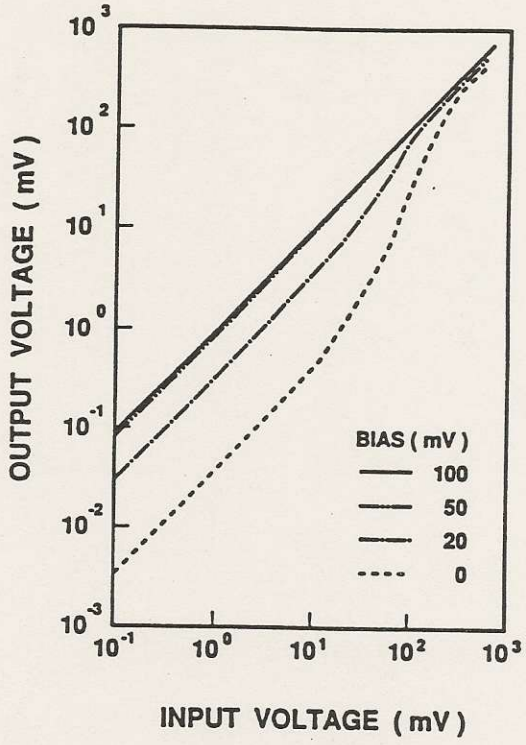


Fig.6 Output voltage VS. input voltage

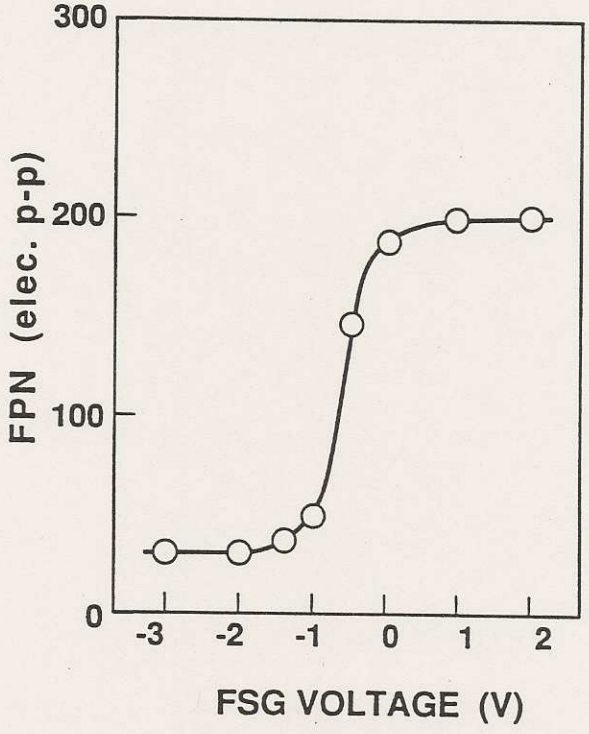


Fig.7 Noise electron VS. read-out gate voltage